Data Bus Deskewing Systems in Digital CMOS Technology

A Thesis
Presented to
The Academic Faculty

by

Amer Hani Atrash

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

School of Electrical and Computer Engineering
Georgia Institute of Technology
May 2004

Data Bus Deskewing Systems in Digital CMOS Technology

Approved by:

Dr. Brian Butka, Advisor (Integrated Device Technology)	Professor Ahmet Erbil
Professor David Hertling, Co-Advisor	Professor Phillip Allen
Professor Vincent Mooney	Professor Jeffrey Davis

Date Approved: 4 May 2004

To my parents, Hani and Nouhad,

my brother Amin, my sister Zeina,

and the memory of Dr. John P. Uyemura.

ACKNOWLEDGEMENTS

I want to express my appreciation to the following people for their help over the past several years. Their support has made my completion of this program possible.

First and foremost, I would like to thank my advisor Dr. John Uyemura for his encouragement and guidance during my undergraduate and graduate work. In addition to technical guidance, Dr. Uyemura's contributions to my personal development have proven invaluable to me over the past years. His advice and support, particularly during my transition to graduate work, helped shape my personal and professional development, even after his passing. All his guidance, advice, and support during the short time I knew him are greatly appreciated.

My appreciation is also extended to Ms. Melba Uyemura. Her advice has helped keep me on the right track, both in completing my degree and transitioning to industry. I am fortunate to have had her support this past year.

I would also like to thank Dr. Brian Butka and Dr. David Hertling who became my advisors after losing Dr. Uyemura. Their advice was critical in guiding my work and allowing a timely completion of my degree.

My gratitude is also extended to my family, whose confidence in me and unwavering support have been a foundation upon which I can always trust.

Finally, I would like to thank all my friends, who contributed in countless ways to my achievements these past years. Their social and moral support allowed me to keep a good attitude through everything that has happened.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

This dissertation presents a study of signal deskewing systems in standard CMOS technologies. The objective of this work is to understand the limitations of deskewing systems as they are applied to modern systems and present new architectures to overcome past limitations. Traditional methods for signal deskewing are explored and the general limitations of these methods are identified. Several new architectures are proposed to address the limitations of previous techniques. The systems will be investigated with regard to minimum resolution, programming time, delay, maximum data rate, full scale range, and duty cycle distortion. Several other effects that are critical to the operation of deskewing systems will also be investigated. These effects include overshoot caused by parasitic package inductance, the impact of capacitive terminations, and the effect of mutual inductance between traces.

To fulfill the requirements of this study, two deskewing systems are implemented in a 0.25 μm process. An open-loop system for deskewing wide data busses and a closed-loop system for deskewing a differential pair of lines are both fabricated. Both systems are found to meet the expected performance metrics, providing validation of the proposed techniques. Use of the proposed architectures allows the limitations of previous methods to be overcome. The remaining work is validated through either analytical techniques, simulations, or both where appropriate.

CHAPTER I

INTRODUCTION

1.1 Motivation

Many modern designs attempt to combine several different functionalities into one system. These functionalities may include processing, memory, specialized interfaces, and dedicated clock generators. These different functions may be combined into a single integrated circuit (IC) or spread among several different ICs. The ICs, in turn, may all be on a single printed circuit board (PCB) or distributed onto several connected boards. Between-chip communication in these systems occurs through metal traces printed onto the boards. The lengths of these traces may vary anywhere from a less than an inch on a small board to more than 10 inches on a large board, such as a PC motherboard. Due to the extremely long length of the traces, the propagation delay of signals across the traces becomes quite significant, particularly for high-speed communication. Differences in trace lengths or variations in trace characteristics can cause skew between a pair of traces. As between chip communication frequencies increase, the skew between traces becomes an increasing percentage of the total system clock period. As clock frequencies scale up, the amount of skew that can be tolerated by these systems decreases. Therefore, low-skew signal transmission is a requirement of modern multi-chip high-speed digital systems. Signal skew between targets in these systems can comprise a significant fraction of a system's timing budget. Excessive skew can result in decreased system clock frequencies or system malfunction. Reducing skew is essential for maintaining high clock frequencies and proper system functionality. The increasing importance of signal skew, the ubiquitous nature of the problem, and the necessity of addressing this problem for high-speed systems provide

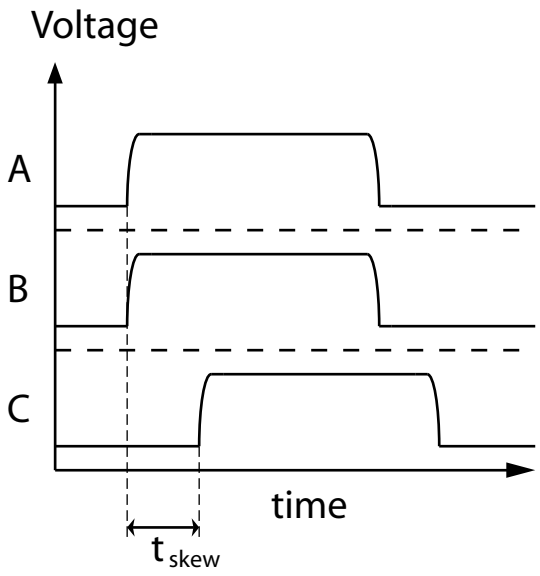

Figure 1: Illustration of signal skew.

the motivation for this work.

In this document, *skew* is used to refer to the time difference between electrical signals. For example, in Figure 1, there is no skew between signals A and B, but there is a skew of t_{skew} between signals B and C. In an ideal sense, the skew will be measured at the trip point of the receiving chip. Many times, however, the receiver trip points will not be known in advance or will not be specified. The deskewing systems described here are designed with as few restrictions on the receiving chip as possible and will not specify or assume any particular trip points. Therefore, skew will be measured at the midpoint of the signal swing for single-ended signals, which is $V_{dd}/2$ for full-rail signal swings. If the signal edge rates are identical, then the skew at the midpoint voltage will equal the skew at any other chosen trip point.

The problem of signal skew arises when trace lengths between two chips are unequal or when process variation makes two PCB traces with identical length support different signal propagation velocities. This is particularly a problem when sending a large number of bits in parallel in a wide data bus, when trying to synchronize a clock signal with a data word, or when trying to send a single clock signal to multiple

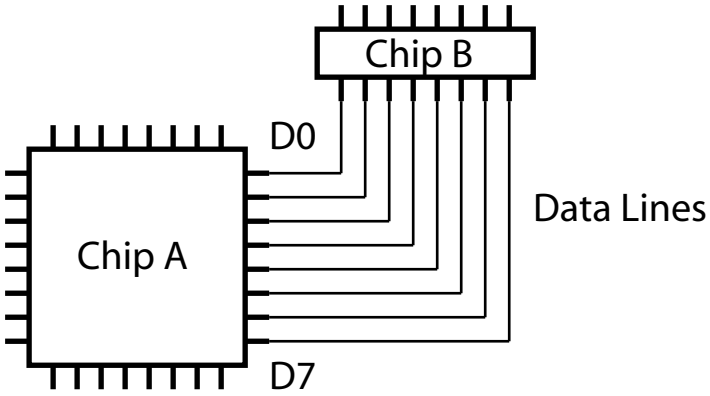

Figure 2: Illustration of a wide data bus where every bit traverses a different length PCB trace.

target chips with identical phase. These situations arise easily in a typical PCB design. Consider the examples shown in Figures 2 and 3. In Figure 2, the transmitting chip, Chip A, attempts to send an eight-bit data word (D0 to D7) in parallel to the receiving chip, Chip B. Because of the orientation of the chips, however, each data bit traverses a different path length. Bit D0 travels the least distance and bit D7 travels the greatest difference. Therefore, if every bit is started simultaneously, they will each arrive at the receiver at a different time. The time difference between the bits is skew that can cut into the system timing margins. If the skew is too great, data transmission errors may result. In addition, attempting to synchronize a clock signal to the transmitted data bits will prove extremely difficult, since every bit and the clock will traverse a different path and arrive at a different time.

The situation shown in Figure 3 represents the case where a single clock-buffer chip attempts to transmit a single clock to several targets with identical phase. Each of the targets, however, lies a different distance from the clock buffer chip. The differences in distance may be very large for a large PCB, such as in a PC motherboard which can easily exceed 10 inches on a side. In this case, the skew between the clock signals at the receivers could easily exceed 1 ns. Elimination of this skew improves synchronization between the chips and helps prevent data transmission errors.

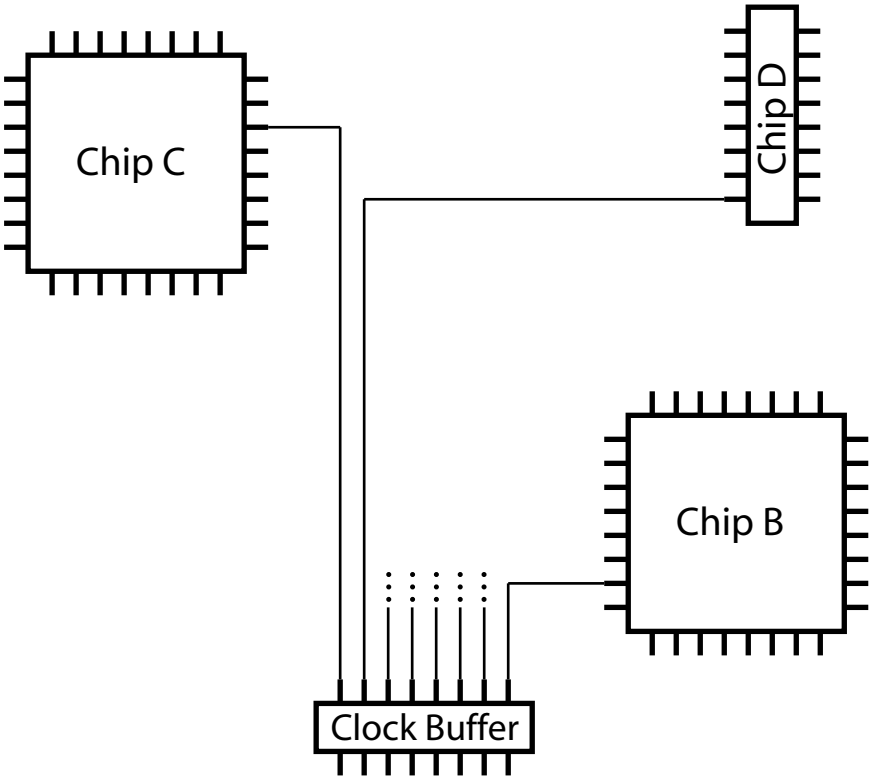

Figure 3: Illustration of a situation where a single clock is distributed to several targets. PCB trace length differences create skew between the clock edges at the receiving chips.

The most simplistic solution to the problem of signal skew is to draw every trace with identical length. In practice, however, this can extremely difficult or impossible to do if there is more than one target chip or if a data bus to one chip is very wide. In addition, random process variation between traces can cause variations in the propagation velocity of signals through the traces. Furthermore, the environment of the traces has a direct impact on signal propagation on the trace. In a multi-bit data bus, the first and last bit may have only one adjacent trace while every other bit will have two adjacent traces. This results in the first and last traces supporting different propagation velocities than the remaining traces.

Ultimately, signal skew can arise in any system, either through differences in trace lengths or environments or simply through random variation in the trace dimensions. These effects can be somewhat reduced through proper PCB design, but cannot

be completely eliminated. As system frequencies scale up, the skew between traces becomes an increasingly significant fraction of the total system period and can become a limiting factor in extremely high-speed designs. Therefore, it is desirable to have a way to automatically compensate for the skew between PCB traces. An ideal system will be able to measure and correct the skew without knowing in advance the lengths or propagation delays through the traces and without requiring any specialized circuitry outside the transmitting chip. Besides skew correction, the system should be otherwise transparent to the rest of the circuitry on the chip.

1.2 Thesis Organization

The goal of this dissertation is to study systems used to eliminate the skew between PCB traces. Previous techniques used to address this problem will be discussed and their limitations will be identified to create a starting point for the research. The research presented here will address the limitations of the previous techniques and demonstrate new methods of signal deskewing. Several new deskewing architectures are proposed which address critical issues in deskewing systems, such as wide data buses and differential signal transmission. These new architectures will be characterized and their limitations will be identified.

In Chapter 2, the principles that provide the basis for the origin of signal skew will be discussed. This is followed by a discussion of previous techniques which attempted to solve the signal skew problem and a highlighting of the shortcomings of these techniques. Chapter 3 presents an open-loop deskewing system for use with wide data busses. The implementation details of this system are presented, along with a characterization and analysis of the system. This chapter concludes with an analysis of the effects of overshoot and capacitive terminations on the deskewing system. In Chapter 4, the limitations of the open-loop system are discussed in detail and design trade-offs of the system are presented. The effects of dispersion and mutual inductance

between traces will also be addressed. A system for deskewing a differential pair of PCB traces is presented in Chapter 5, along with a characterization and analysis of the system. Chapter 6 discusses a deskewing system that measures propagation delay by sensing the current through the output driver. The implementation details of this system are presented along with a discussion of the advantages and disadvantages of this approach. A comparison of the techniques presented in Chapters 3 and 6 will also be performed. Finally, in Chapter 7, a brief summary of the work is presented along with a discussion of the major contributions of the work and potential future directions for further research.

CHAPTER II

BACKGROUND

2.1 Origin of the Problem - A Circuit Viewpoint

The origin of signal skew from waves travelling down transmission lines lies in the effects of the physical characteristics of the lines. For this analysis, the transmission line is considered to be a series of line segments of infinitesimally small length (dz). Each segment is modelled using a series resistance (R), series inductance (L), shunt conductance (G) and a shunt capacitance (C), where each of the quantities is defined per unit length of the line. The two-port model using these components is shown in Figure 4.

In general, this line can be characterized using Kirchhoffs Voltage and Current Laws as follows.

$$v(z,t) - Ri(z,t)dz - L\frac{\partial i(z,t)}{\partial t}dz + v(z+dz,t) = 0 \tag{1}$$

$$i(z,t) - Gv(z+dz,t)dz - C\frac{\partial v(z+dz,t)}{\partial t}dz - i(z+dz,t) = 0 \tag{2}$$

These equations can be solved to demonstrate that a wave will travel through the

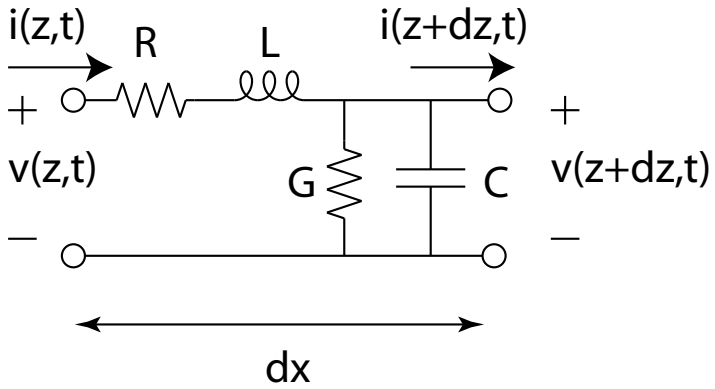

Figure 4: Two-port transmission line model.

line with a finite velocity given by Equation 3 [23].

$$v_p = \frac{1}{\sqrt{LC}} \tag{3}$$

This result indicates that a voltage wave will travel at a finite velocity through any medium. In addition, this velocity will be less than the speed of light for any medium other than free space. Therefore, the length of time required for a signal to traverse a particular path is directly proportional to the length of that path. If two signals are started simultaneously down two microstrip lines having the same physical dimensions but different length, then the wave propagating down the shorter line will arrive earlier than the wave propagating down the longer line. In addition, variations in L or C will also cause variations in v_p. This will cause two lines with identical lengths to have different propagation delays [11]. These effects are the origin of signal skew between PCB traces.

2.2 Time Domain Reflectometry Basics

This section presents some basic characteristics of transmission lines that will be of relevance to the work presented here. More detailed descriptions of transmission line behavior are widely available in literature [16, 20]. The basic setup is illustrated in Figure 5. This consists of an ideal driver with impedance R_s, an ideal transmission line with impedance Z_o, and a load of Z_L. When the switch closes, a voltage pulse is sent propagating down the line. The magnitude of this pulse (the incident wave) is

$$V_{inc} = V_s \frac{Z_o}{R_s + Z_o} \tag{4}$$

If the driver and trace impedances are matched (i.e. the impedances are equal) then V_{in} will equal $V_{dd}/2$. This pulse propagates down line with a velocity given by Equation 3 until it reaches the termination Z_L. At the termination, a reflected wave is created which propagates back toward the source with identical velocity. The

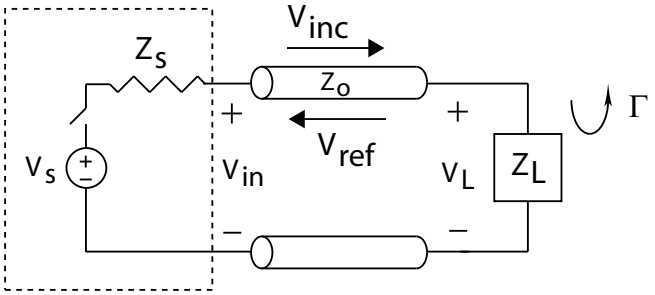

Figure 5: Basic transmission line setup.

magnitude of this reflected wave will be given by

$$V_{ref} = \Gamma V_{inc} \tag{5}$$

where

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{6}$$

The total voltage at the receiver is equal to the sum of the magnitudes of the incident and reflected waves. The reflected wave will reach the source and may be reflected again if the driver and line impedances are mismatched (or not equal). For simplicity, assume that the driver and trace are matched, so only a single wave propagates forward through the line and a single reflection propagates backwards through the line.

The effects of several terminations will now be addressed. The first case is for an open circuit load ($Z_L = \infty$). In this case, $\Gamma = 1$ and the magnitude of the reflected wave equals the magnitude of the incident wave. The voltage at the receiver will then equal twice the magnitude of the incident wave. If the driver and trace are matched, then $V_{inc} = V_{dd}/2$ and the voltage at the receiver will equal V_{dd}. This case is illustrated in Figure 6 where the propagation delay through the transmission line is equal to t_d.

The second case of interest is for a short circuit load ($Z_L = 0$). In this case, $\Gamma = -1$ and the magnitude of the reflected wave is the same as the incident wave, but opposite sign. When this occurs, the voltage at the receiver remains at 0. This

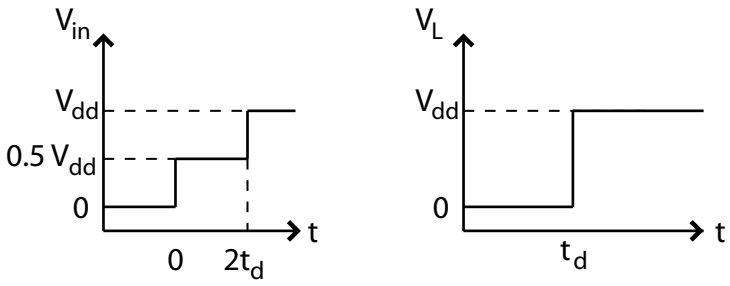

Figure 6: Transmission line illustration for an open-circuit load.

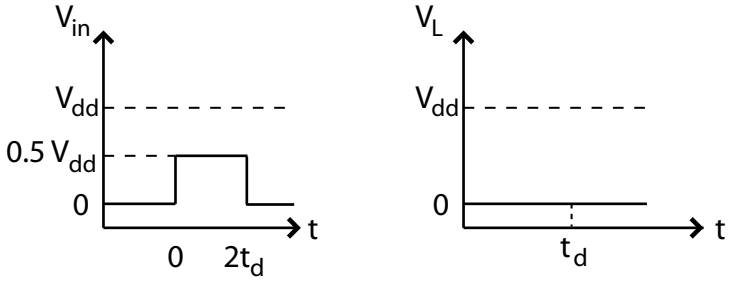

Figure 7: Transmission line illustration for a short-circuit load.

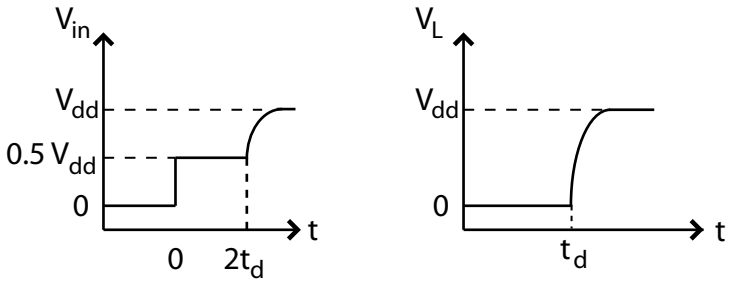

Figure 8: Transmission line illustration for a capacitive load.

case is illustrated in Figure 7.

The final case of interest here is for a capacitive load. In this case, Z_L is purely imaginary. The magnitude of the reflection coefficient is still 1, but the capacitor introduces another effect. The edge rate of the reflected signal will decrease as the capacitor charges. This is illustrated in Figure 8. The voltage at the input of the transmission line will eventually charge to V_{dd}, but will require more time than the case with an open-circuit load.

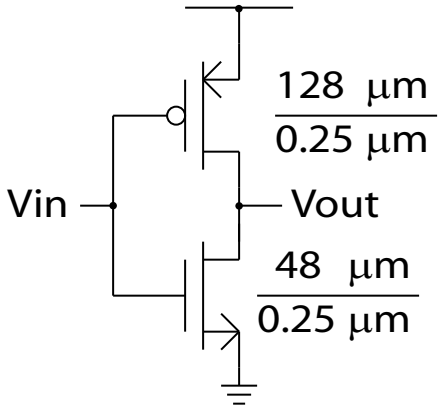

Figure 9: Output buffer schematic with device dimensions annotated.

2.3 Output Buffer

The circuit setup in Figure 5 uses an ideal 50 Ω driver. In an application, any of a variety of techniques could be used to implement this driver. As long as the driver has the appropriate equivalent output impedance, use of an idealized model does not introduce too great an error. In the work presented here, an appropriately scaled inverter provides a 50 Ω driver. This circuit is illustrated in Figure 9 with the device dimensions as indicated. The output impedance of this circuit is not constant and can vary be several orders of magnitude as the input voltage varies. The devices are scaled to give an equivalent 50 Ω impedance for the regions of primary interest - particularly, when the input is at 0 V or V_{dd}. Simulation results of the equivalent output impedance of the driver are shown in Figure 10. When the input voltage is switching, the output impedance changes from 50 Ω for $V_{in} = 0$ or $V_{in} = V_{dd}$ to nearly 5 kΩ for $V_{in} = 1.25\,V$. However, the most important state is the state of the buffer when the reflection returns to the buffer from the end of the line. At this point, the input will have completed its switch and will be stable at 0 V or V_{dd}. If the input is still switching, then the round-trip propagation delay through the PCB trace is less than the rise time of the driver input. In this case, the PCB trace is very short and will not need deskewing.

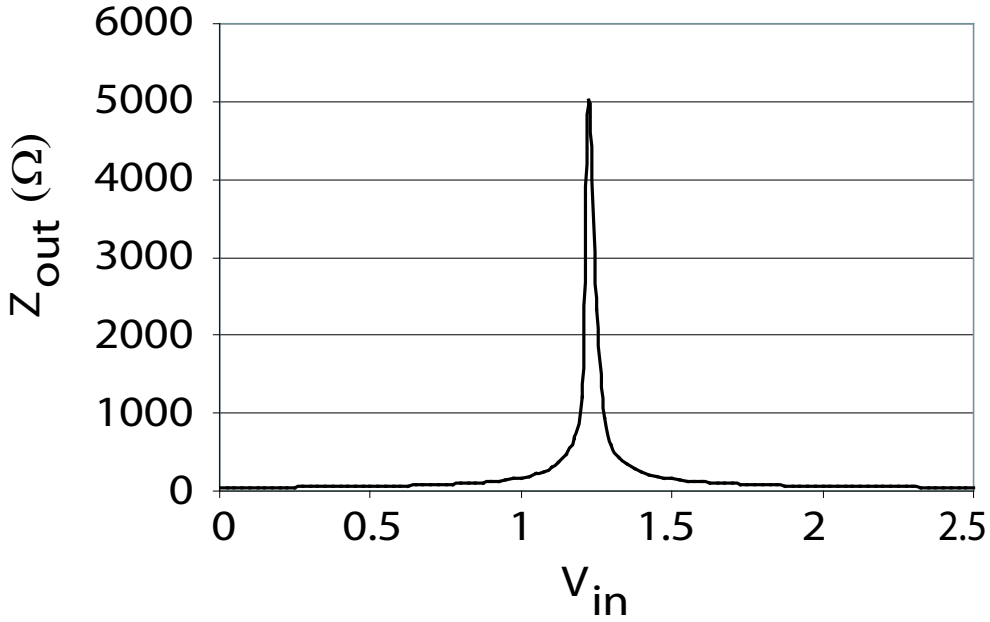

Figure 10: Output buffer equivalent impedance.

2.4 Zero-Delay Buffering

The current techniques for correcting signal skew caused by propagation through a transmission line focus on clock distribution between chips or within a single chip. Typically, this correction is performed using a technique similar to zero-delay clock buffering. Zero-delay buffering takes an input clock and creates a buffered version of the clock that is exactly in phase with the incoming clock. These techniques attempt to eliminate the skew that ordinarily exists between the input clock and the buffered, internal clock. While it is not possible to create buffering with zero delay, the effect of zero delay is achieved if the phases of the incoming and buffered clocks are exactly the same. The delay from the input to the buffered output, in this case, will be an integer multiple of the clock period [13, 39]. These systems require that the input be a periodic waveform and will not work for nonperiodic signals. The basic architecture of a zero-delay buffer is shown in Figure 11.

This system is simply a delay locked loop (DLL) that has been set up around the clock drivers. The system consists of a variable delay cell, phase comparator, delay

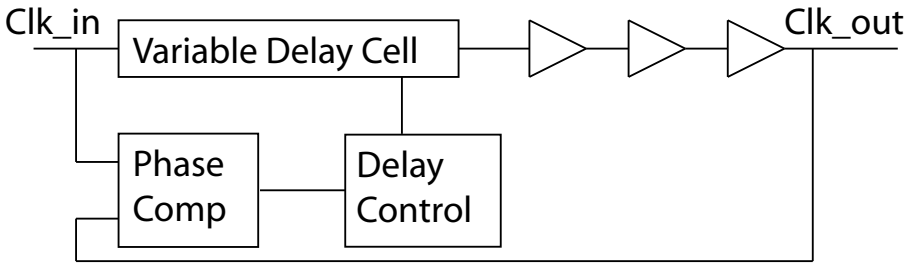

Figure 11: Zero-delay buffer.

control, and the clock drivers. The delay control block is typically implemented as a charge pump and loop filter. The phase comparator compares the phases of the input and output clocks. If the clocks are not in phase, then the phase comparator adjusts the delay of the variable delay cell until the clocks are in phase. The ultimate goal of this circuit is to compensate for some unknown delay (in this case the delay through the clock drivers) by controlling the delay through the variable delay cell.

2.5 Delay Locked Loop Solutions

Several methods for eliminating signal skew have been presented in literature. These skew-compensating circuits tend to follow one of the two basic DLL architectures shown in Figures 12 and 13 [19, 21, 39, 40].

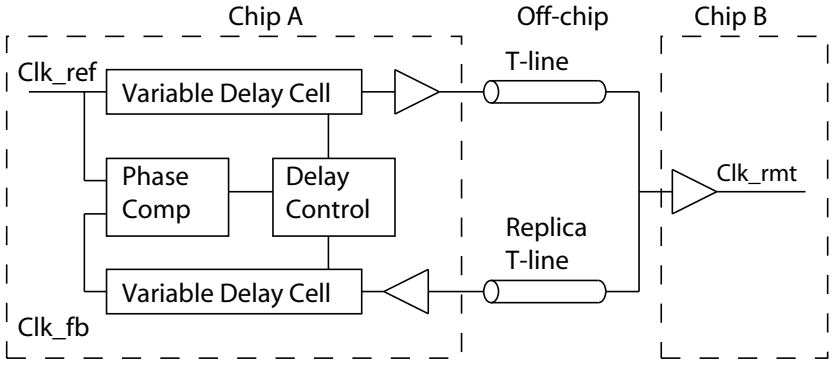

Figure 12: Clock deskew buffer architecture 1.

In these circuits, the phase comparator controls the delay through the voltage controlled delay lines (VCDL's) until the feedback clock (Clk_fb) has the same phase as the reference clock (Clk_ref). If Clk_fb arrives before Clk_ref, the delay through the

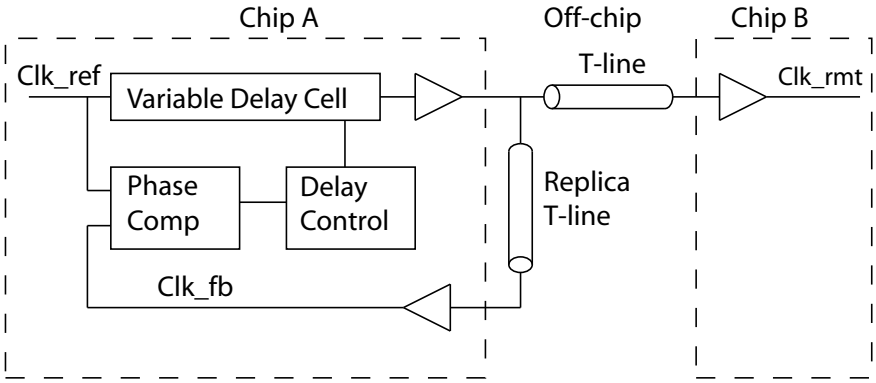

Figure 13: Clock deskew buffer architecture 2.

VCDLs is increased. If Clk_ref arrives before Clk_fb, the delay through the VCDLs is decreased. Like the zero-delay buffer, these systems are implementations of delay-locked loops. The accuracy with which the delay can be controlled depends on several factors, the most important being the phase detectors, VCDLs, and the degree of matching between the transmission line and the replica line. The VCDLs and corresponding control circuitry are built using either analog or digital techniques, each having its own advantages and disadvantages. Correct operation of this system assumes that the off-chip transmission line and replica transmission line are exactly matched. Any mismatches in the physical characteristics of these lines, such as random variations in the width or thickness of the lines or thickness of the dielectric substrate, will cause a phase mismatch at the receiver.

2.6 Delay Lines

Design of the VCDL is critical to overall system performance in these DLL systems. The characteristics of the line will set the granularity of the variable delay, which is a limiting factor in achieving minimum skew, and will determine the nature of the control circuitry. In general, a VCDL will be one of two types, those having analog control voltages and those having a digital control word. An analog controlled DLL [3, 21, 34, 40] uses a charge pump and loop filter to control the VCDL. These

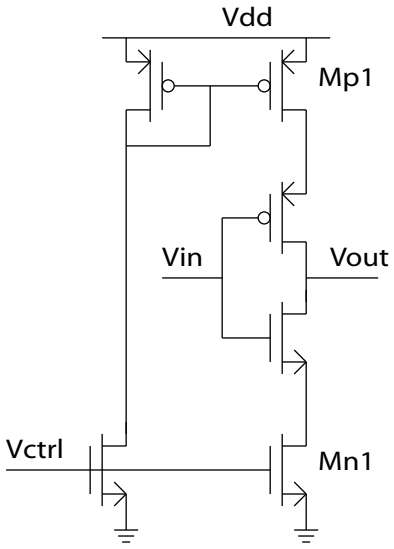

Figure 14: Current starved inverter stage.

systems can achieve a theoretically continuous range of delays from the VCDL and therefore provide perfect skew correction, however, in practice, the resolution of these systems will be limited by the charge pump and noise on the control line. In addition, an analog-controlled VCDL will have a smaller tuning range than a digitally-controlled VCDL. A digitally controlled VCDL [7, 35, 39] uses a counter or register to provide the control word. These systems will produce only quantized delays, but have less noise sensitivity and larger tuning range than the analog-controlled VCDL's. A more detailed discussion of both types of VCDLs follows.

2.6.1 Analog Control Delay Lines

Delay lines using analog controls are used extensively in literature. The two most common types of delay cells are the current starved inverter (CSI) [3, 17, 34] and the variable RC delay stage [3, 17, 21]. To make a VCDL with acceptable tuning range, several individual stages are placed in series. The number of cells will be determined by the maximum delay necessary from the VCDL. Using more stages increases the tuning range, but also increases the minimum delay through the VCDL. A schematic of a basic CSI stage is shown in Figure 14.

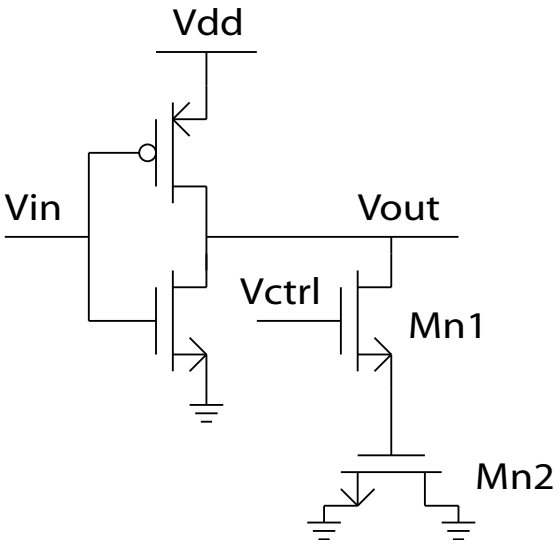

Figure 15: RC delay stage.

In this cell, V_{out} is computed as the inverse of V_{in} as in a standard CMOS inverter. However, the current required to swing the output node voltage is restricted by transistors Mn1 and Mp1. The voltage V_{ctrl} regulates the equivalent resistance through Mn1 and Mp1 through the current mirror. If V_{ctrl} is large, then the equivalent resistances of the transistors will be small and the output can switch quickly, giving a small propagation delay. If V_{ctrl} is small, then the equivalent resistances of Mn1 and Mp1 will be large and the delay through the gate will be large. Delay lines built using this technique are reported to have resolutions of less than 100 ps in a 0.35 μm process [40] and 30 ps in a 0.5 μm process [34]. In principle, the resolution of the delay line is not limited by the CSI stage, but rather by the resolution of the control circuitry and other noise sources.

The schematic of the variable RC delay cell is shown in Figure 15. This cell operates logically like a standard CMOS inverter, giving V_{out} as the complement of V_{in}. However, the effective load on the cell is controlled by V_{ctrl}. The device Mn2 acts as a load capacitor and could be replaced by another type of capacitor, if desired. The device Mn1 acts as a resistor. Setting the value of V_{ctrl} adjusts the equivalent resistance of Mn1 and hence the RC time constant of the network. Other delay lines

exist that have analog control voltages. These other schemes rely on adjusting the delay through a stage by changing the bias current available to that stage [37] or by applying a current-starving technique to a Schmitt Trigger circuit [40]. Regardless of the particular technique, these delay lines all have similar characteristics. An analog control voltage allows for theoretically arbitrarily small adjustments to be made to the delay of a single cell, allowing for a continuous range of available delays. The resolution of an analog-controlled delay line will then be limited by the resolution of the control circuitry and noise on the control line. In addition, storing an analog voltage can be difficult in the presence of noise sources. As a result, analog-controlled DLLs tend to be better suited for use in a clock deskewing system, where a purely periodic signal can be used to constantly update the control voltage as environmental conditions change or noise causes shifts in the control voltage.

2.6.2 Digital Control Delay Lines

Digital control is implemented in a variety of ways, including using digital words, counters, or shift registers. These digital techniques work, in principle, as illustrated in Figure 16 [7].

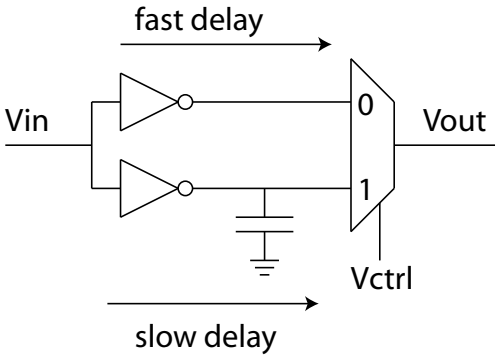

Figure 16: Digital delay stage.

In this circuit, the control voltage is used to choose between either the slow or fast path through the cell. By controlling the size of the capacitor, the delay difference can be determined during design. A VCDL is created from these cells using the

architecture in Figure 17.

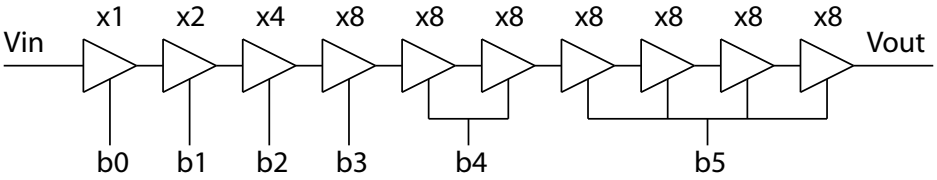

Figure 17: Digital VCDL architecture.

In this circuit, the multiplier indicates the number of capacitors added to the slow path. In [7], this design is reported to achieve a unit delay of 160 ps and a tunable range of 10 ns, but has an offset delay of 9.2 ns in a 0.25 um process. An advantage of this technique is that the architecture can accept a digital word as a control signal and automatically weights the bits to achieve the correct linear combination of unit delays, allowing the control circuitry to be as simple as a counter.

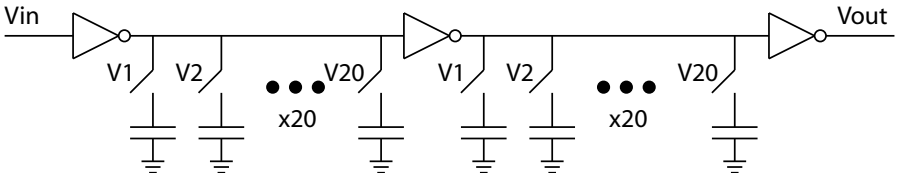

Figure 18: Alternate digitally controlled delay line stage.

Another technique using digital control involves changing the load on a node in the circuit using transmission gates [35], as shown in Figure 18. By selecting the number of capacitors that are switched into the signal path, the delay of the VCDL can be changed. In the literature, this circuit is controlled using a 20-bit delay control register, with every bit having the same weight. The output is driven by a push-pull style driver. This architecture provides a total of 20 linearly spaced steps, giving a maximum delay range of 170 ps in 8.5 ps increments in a 0.18 μm process.

Digitally controlled VCDLs have several advantages over analog controlled VCDLs. The most important are increased noise immunity on the control lines, wider tuning range, and simpler control circuitry. In addition, storing a digital control word can

be trivially achieved by using a simple register. Unfortunately, these benefits come at the expense of larger offset delay and quantization in the available delays.

2.7 Synchronous Mirror Delay

Another major technique related to signal deskewing is synchronous mirror delay (SMD). This technique is used to create a zero-delay buffer, where the output clock is a buffered version of the input clock and exactly in phase. The basic SMD architecture is shown in Figure 19 [25, 29].

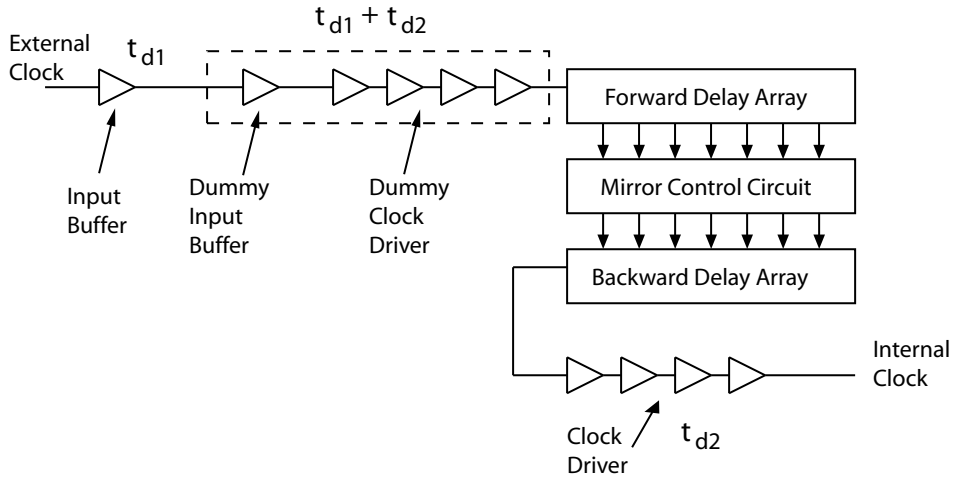

Figure 19: Basic synchronous mirror delay architecture.

This system consists of an input buffer with delay t_{d1}, forward delay array (FDA), backward delay array (BDA), mirror control circuitry, clock driver with delay t_{d2}, and a dummy input buffer and clock driver with total delay $t_{d1}+t_{d2}$. A clock pulse of period T_{clk} input to the system travels through the input buffer and dummy input buffer and dummy clock driver and a time period of T_{clk}-t_{d1}-t_{d2} through the FDA. At this point, a second clock pulse locks in the position of the first pulse. The first pulse then travels back through the BDA a time period of T_{clk}-t_{d1}-t_{d2} and through the clock driver. The total delay experienced by the pulse is described by the following

equation, as defined in [33].

$$t_{d1} + (t_{d1} + t_{d2}) + (T_{clk} - t_{d1} - t_{d2}) + (T_{clk} - t_{d1} - t_{d2}) + t_{d2} = 2T_{clk} \quad (7)$$

It can be seen that the total delay through the system is equal to twice the period of the clock, indicating that the buffered clock will be exactly in phase with the input clock. Thus, deskewing has been achieved in only two clock cycles.

This system can correct for skew between the input clock and the buffered internal clock to within the delay increment of the delay arrays. This increment is typically the delay through a NAND gate and inverter in series. Results have been reported in literature using interleaving [32,33] or analog techniques [4,15,26,28,29] to reduce the delay to less than one unit delay. These systems produce results that are on the same order as those of the DLL's discussed previously, but requires fewer cycles to achieve a lock. The SMD technique is used only for deskewing clock inputs and will deskew only purely periodic signals.

2.8 Time Domain Reflectometry

Techniques have been reported in literature [1,19] utilizing time domain reflectometry (TDR) techniques. In these systems, a pulse is sent down the PCB trace. If the trace is underdamped (i.e., the line termination has a high impedance compared to the characteristic impedance of the line), then the pulse will be reflected at the receiving chip and return to the transmitting chip. The reflected pulse is detected using an appropriately tuned comparator. These systems also implement a DLL around the PCB trace and will only deskew purely periodic signals. Use of TDR techniques eliminates the need for dummy PCB traces. However, the magnitudes of the transmitted and reflected pulses will depend on the relative impedances of the driver and PCB trace. Mismatches between these impedances can cause the deskewing systems to malfunction.

2.9 Remarks

Several techniques have been used in literature to deskew signals sent between chips. Although these techniques have proven effective in the past, they all possess certain limitations, as follows:

- Skew correction is applied only to individual signals and cannot be used to deskew digital words.
- A DLL requires a large number of cycles to achieve a lock.
- These techniques deskew only purely periodic signals and will not work for non-repetitive signals, as in an arbitrary data stream.
- These techniques are used only for single-ended signals and cannot be applied to differential systems where the PCB traces will be terminated with a resistor.
- Dummy lines are frequently used to estimate delay through the signal lines, consuming extra package pins and board space and introducing error resulting from mismatch from the signal lines.

CHAPTER III

AN OPEN-LOOP DESKEWING SYSTEM

3.1 System Description

The research presented here has sought to resolve several of the limitations of previous designs. The technique presented in this chapter is an open-loop system that calculates the delay correction required for each line in a wide data bus and applies the correction in a single cycle. The result can then be used to deskew both repetitive and nonrepetitive signals on all the lines. Time domain reflectometry is used to measure the length of each line, eliminating the need for dummy lines and the potential mismatch between the dummy and signal lines. This new technique can be extended to deskew any number of signals sent in parallel between two chips.

In an application, it is expected that a system's characteristics may change over a period of time as the system power supply voltage or temperature shift due to external factors. In this case, the open-loop system could be reprogrammed periodically to track changes in system characteristics that may have occurred. Since the system can be programmed in a single cycle, the overall effect on system performance will be minimal in these cases. In practice, the system is in a closed-loop state while being programmed, but runs in open loop at all other times. In the context of this thesis, however, this system will always be referred to as an open-loop system to distinguish it from other systems which only operate in a closed-loop manner.

3.1.1 System Architecture

The block diagram of the open-loop architecture is shown in Figure 20. It consists of a VCDL, subtractor, output buffer, counter, and Schmitt trigger circuit for each

output line, as well as a single oscillator and a combinational logic block for the entire system. All these components are created using static CMOS techniques. To measure the round-trip delay through each PCB trace, the system sends a pulse down each line and waits for the reflection. If the end of the line is underdamped, then the transmitted pulse will be reflected back toward the transmitting chip. The number of edges produced by a three-stage ring oscillator during the period between when the pulse is first sent down the line and when the reflection returns to the transmitting chip is counted using a set of counters and is directly proportional to the round-trip delay through the line. The maximum delay is computed using standard CMOS comparators and will correspond to the bit with the slowest PCB trace. The difference between each line's delay and the maximum delay is the delay difference that must be added to that line to match its delay to the slowest line. This difference is calculated using a CMOS subtractor and is the control word for the binary-weighted VCDL. The slowest trace is typically the longest trace in cases with different length lines or the trace with the greatest capacitance and inductance per unit length for equal length traces. The correction for the slowest line will be 0. The delay measurement process results in quantized values for each line. Therefore, delay correction will also occur in a quantized manner, which is best implemented by a digitally controlled VCDL.

3.1.2 System Operation

The delay from the data input to the receiving chip for the ith line, $T_{data,i}$, is given by Equation 8.

$$T_{data,i} = T_{VCDL,i} + T_{buf} + T_{PCB,i} \tag{8}$$

where $T_{VCDL,i}$ is the delay through the VCDL for line i, T_{buf} is the delay through an output buffer and is assumed to be identical for every line, and $T_{PCB,i}$ is the delay through the PCB trace connecting the ith line with the receiving chip. When all the

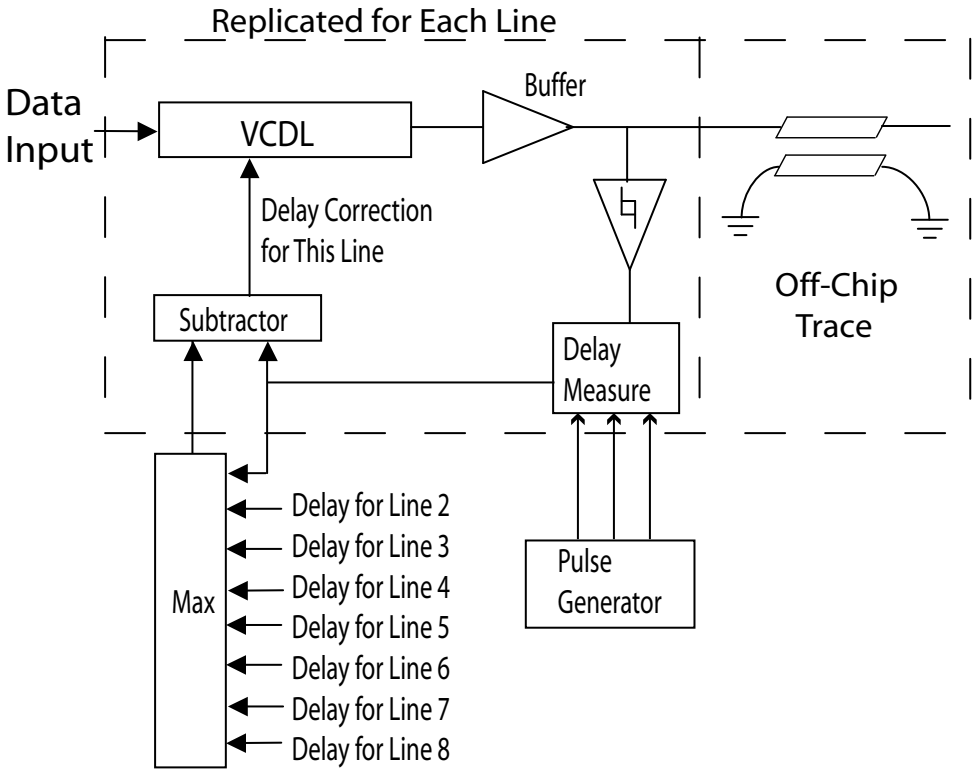

Figure 20: Data bus deskewing system architecture.

lines are deskewed,

$$T_{data,i} = T_{data,j}|_{\forall j \neq i} \tag{9}$$

The delay correction that is programmed into each VCDL is given by

$$T_{VCDL,i} = T_{offset,VCDL} + T_{PCB,max} - T_{PCB,i} \tag{10}$$

where $T_{offset,VCDL}$ is the offset delay of the VCDL and $T_{PCB,max}$ is the maximum delay (the delay through the slowest PCB trace). After programming, the delay for each line will be

$$T_{data,i} = (T_{offset,VCDL} + T_{PCB,max} - T_{PCB,i}) + T_{buf} + T_{PCB,i} \tag{11}$$

which reduces to

$$T_{data,i} = T_{offset,VCDL} + T_{PCB,max} + T_{buf} \tag{12}$$

At this point, it can be seen that the condition of Equation 9 has been satisfied and

the total delay for each bit has become independent of the propagation delay through the PCB traces.

The assumption made above that every output buffer has identical delay may not always hold. In practice, every buffer will exhibit a slightly different delay because of process or temperature variations. These variations will, however, not create a problem. Any difference in buffer delays for a given line will appear to the system as variations in the PCB trace delays since the delay measurement process includes the delay through the buffers as well as the traces. Therefore, any differences in buffer delays will be measured by the system and corrected.

3.2 Implementation

This section details an implementation of the open-loop deskewing system just described. The components discussed include the reflection detectors, delay measurement block, oscillator, and VCDL, as these represent the most critical components of the system. This will be followed by a presentation of the simulation results of this implementation. The design of the counters, adders, and digital comparators is achieved through standard static CMOS techniques and will not be discussed here.

3.2.1 Reflection Detection

A CMOS Schmitt trigger is used to detect the reflected pulse [38]. This circuit has been chosen because it has a well controlled trip point, low input capacitance, and a fast switching characteristic. Process variation will cause the trip point to shift, but simulation across several process and temperature corners has verified that the trip point stays within an acceptable range, as shown in Figure 21. The simulation results indicate that the trip point shifts less than 80 mV across all process corners and less than 40 mV due to temperature variations for a particular process. The circuit is tuned to have a forward trip point that is greater than the magnitude of the transmitted pulse and less than the magnitude of the reflected pulse. Therefore,

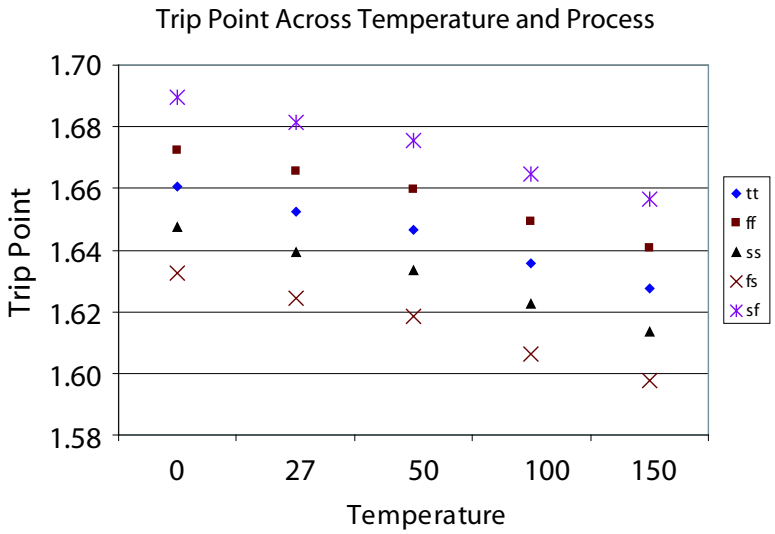

Figure 21: Trip point distribution across several temperatures and process corners.

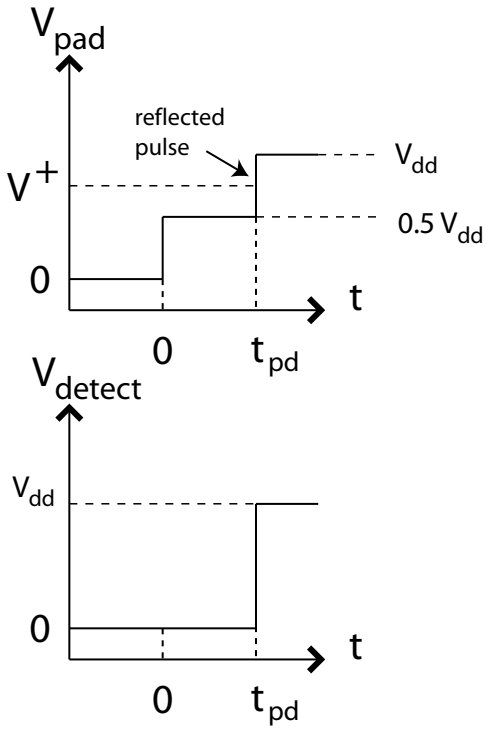

Figure 22: Time domain illustration of reflection detection.

the Schmitt trigger output will trip only when the reflected pulse is detected and not when the forward travelling pulse is sent onto the line. This transient behavior is illustrated in Figure 22. In a 2.5 V process where the line driver impedance is matched to the PCB trace impedance, the trip point is set to be 1.65 V. The forward

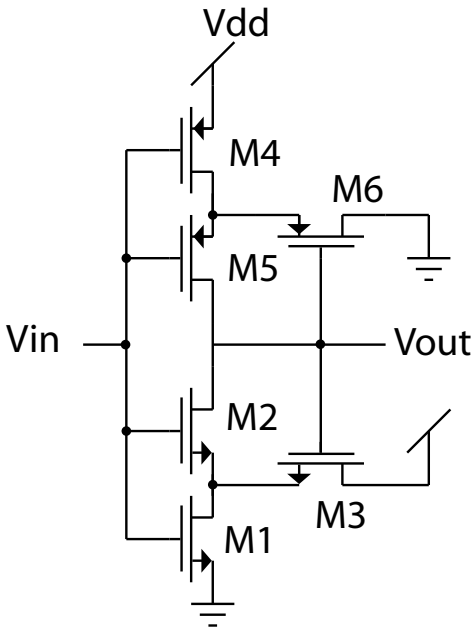

Figure 23: Schmitt trigger circuit.

trip point voltage is given by Equation 13 [38] and will be set predominantly by the relative aspect ratios of devices M1 and M3. The schematic of the Schmitt trigger circuit is shown in Figure 23 and is a standard static CMOS implementation [38]. The circuit requires only six transistors and no DC bias current. Since this circuit is designed to detect the reflected waveform, its input must be tied to the output node of the chip. The input capacitance of the Schmitt trigger will therefore also be added to the total capacitance seen at that node. That capacitance, however, will be dominated by the parasitic capacitance of the package. Therefore, the contribution of the detector will be very small by comparison and can typically be ignored.

$$V^{+} = \frac{V_{DD} + \sqrt{\frac{\beta_{n1}}{\beta_{n3}}} V_{Th}}{1 + \sqrt{\frac{\beta_{n1}}{\beta_{n3}}}} \tag{13}$$

3.2.2 Delay Measurement

The block diagram illustrating the delay measurement technique is shown in Figure 24 where the pulse oscillator in the dashed box is a simple three-stage ring oscillator.

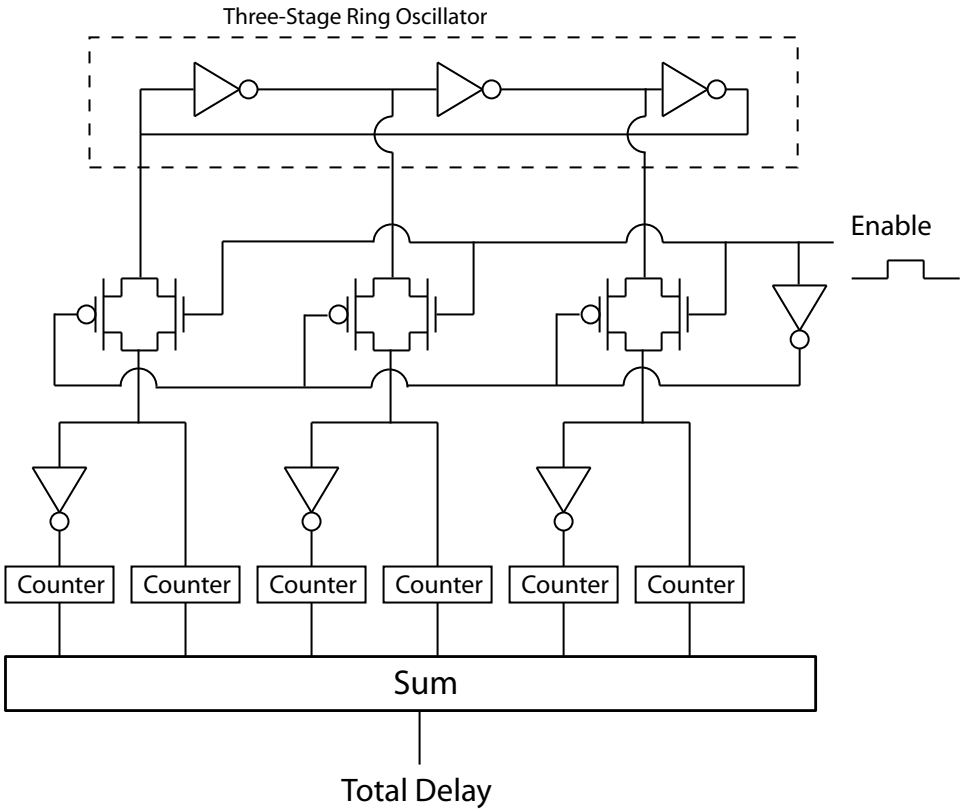

Figure 24: Delay measurement block.

Each phase of the clock is passed through a transmission gate. The gate is controlled by the signal from the detector, such that the transmission gate only passes signals between when the pulse is first sent down the line and when the reflection is detected. During this time, every edge produced by the oscillator will be counted and the total number of edges will be determined. The counters will increment after receiving a rising edge followed by a falling edge. Receiving only one edge will not cause an output transition. In this manner, the rising and falling edges of the oscillator can be discriminated.

Since every edge produced by the three-stage oscillator can be counted, the minimum delay measurement that can be achieved is equal to one sixth the oscillator period. In addition, this results in quantization error in the delay measurement. Only delays in increments of one sixth the oscillator period can be measured. This is the fundamental measurement limitation of the system. Delays that are less than the

delay through a single stage of the oscillator cannot be measured. Using an oscillator with a smaller stage delay will result in improved system performance. Using an oscillator with a greater number of stages will not change the measurement resolution if the stages have the same delay. If the signals on the PCB traces experience a one-way delay of t_d and the oscillator runs with a period T, then the width of the counters, N_{count}, should be at least

$$N_{count} = \lfloor log_2 \left(\frac{2t_d}{T} \right) \rfloor \tag{14}$$

The total delay will then have a minimum width given by

$$N_{Total} = \lfloor log_2 \left(\frac{12t_d}{T} \right) \rfloor \tag{15}$$

The oscillator in this implementation is designed to operate at 2.22GHz (T=450 ps), resulting in a minimum measurement resolution of $T/6 = 75$ ps. To allow measurement of lines up to 10 inches in length ($t_d \approx 1.6ns$), the width of the counters must be at least three bits and the width of the total delay must be at least six bits.

The oscillator in this implementation is not synchronized to the output signals. Therefore, there will exist an offset in every delay measurement. Since the delay measurement circuitry for each line runs from the same counter, however, this offset will be identical for each line. The delay correction is calculated as the difference between two delays, resulting in elimination of the offset.

3.2.3 Oscillator

Since the oscillator stage delay sets the minimum measurement resolution of the system, a high speed oscillator is necessary to achieve good system performance. For this implementation, a differential three-stage ring oscillator with a multi-feedback loop architecture is used. The oscillator architecture is shown in Figure 25 [31]. The multi-feedback loop architecture uses auxiliary feedback loops inside the main loop, driving the stage delay to less than that of a simple static CMOS inverter. Use of this architecture requires oscillator stages having two sets of differential inputs. This second set

of inputs switches before the primary input pair, speeding up signal transitions. The schematic of each oscillator stage is shown in Figure 26 [9]. These stages are 4-input differential delay cells. These stages are created by taking a standard saturated-type delay cell and adding a second set of differential inputs. Saturated type delay cells involve rail-to-rail signals and full switching of the FET's in the stage. Overall, they provide better noise performance than unsaturated-type ring oscillators because some of the transistors are periodically turned off, reducing the effect of thermal noise.

The regenerative properties of the latches speed up the signal transitions, improving both the oscillation frequency and the noise performance of the oscillator. Although the regenerative element in the stage sharpens the signal transitions, it may slow down the oscillation if the feedback is too strong. Making the feedback too weak, however, may reduce the gain of the stage below the minimum value required to start oscillation. The sizing of transistors in this stage is therefore critical for obtaining the desired performance with stable characteristics.

This stage has a rail-to-rail output, allowing it to be directly interfaced to standard CMOS digital circuits. The signal outputs are taken from the positive outputs. To maintain symmetry, identical dummy loads are placed on the negative outputs.

The VCDL stages are designed before fabrication to provide specific delays that are a set fraction of the oscillator period. For ideal operation of the system, the oscillator should have a period of 450 ps. Shifts in the period away from this value will result in the VCDL delay stages providing incorrect delays. To ensure the the oscillator can always run at the correct frequency, the stages can be tuned using the $V_{control}$ signal. This control voltage sets the strength of the feedback in the latching elements. Simulation results show a tuning range of the oscillator from 1 GHz to 2.4 GHz.

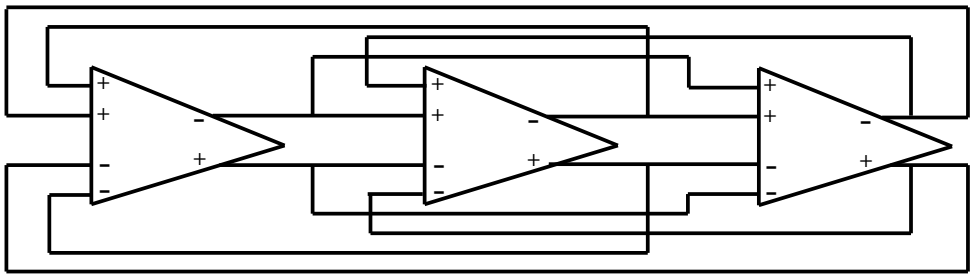

Figure 25: Oscillator architecture.

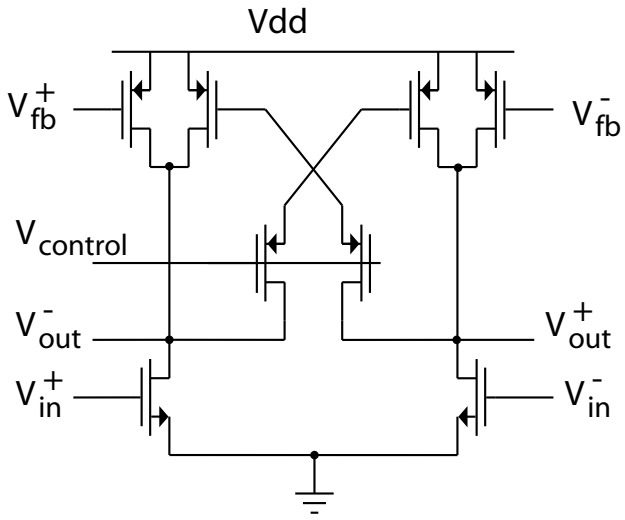

Figure 26: Oscillator stage.

3.2.4 Voltage Controlled Delay Line

Because of the quantization in the measurement process, a delay line that produces quantized delays lends itself directly to the system. The digitally controlled VCDL is implemented using a series of binary weighted blocks. Figure 27 shows the structure of the VCDL where the multiplier shown indicates the weight of the corresponding block [7]. Since the delay measurement process measures the round-trip delay through the trace, the minimum correction required will be half the minimum measurable delay. The lowest order block will therefore produce a delay of one twelfth the oscillator period. For this implementation using a 2.22 GHz oscillator, the minimum delay correction is 450 ps/12 = 37.5ps. This is the minimum delay correction that can be achieved. The schematic of each delay stage is shown in Figure 28. The difference

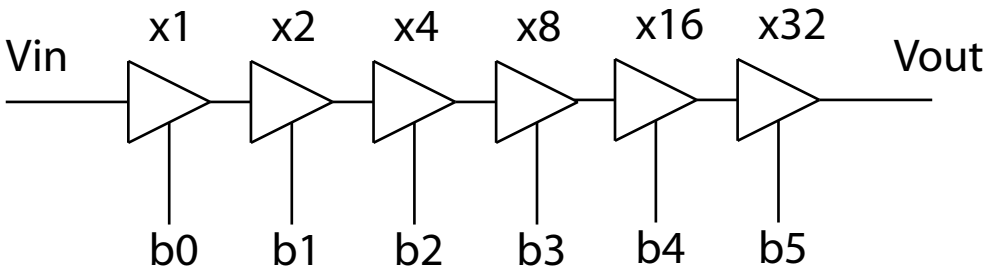

Figure 27: VCDL architecture.

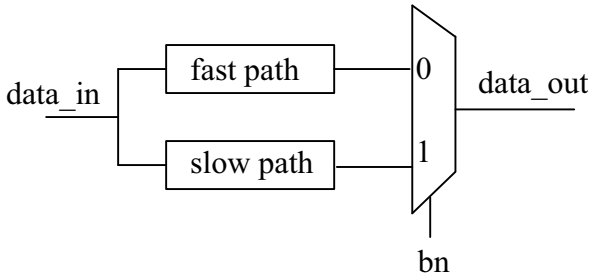

Figure 28: VCDL stage.

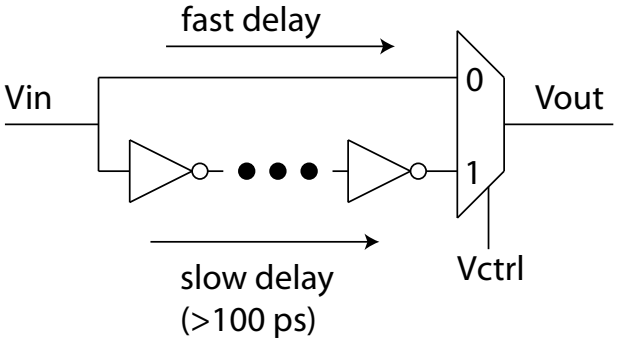

Figure 29: VCDL stage for large delay differences.

in delay between the slow path and the fast path is the delay correction provided by that stage. For long delays, a sufficient even number of inverters is placed in series in the slow path and a short is used as the fast path, as shown in Figure 29. For small delays (less than 100 ps), two inverters are placed in each path and additional capacitance is added to the slow path to set the delay difference as required, as shown in Figure 30. Since an even number of inverters is always used in the signal path, the number of low-to-high transitions will equal the number of high-to-low transitions, minimizing duty cycle distortion of signals propagating through the VCDL [7].

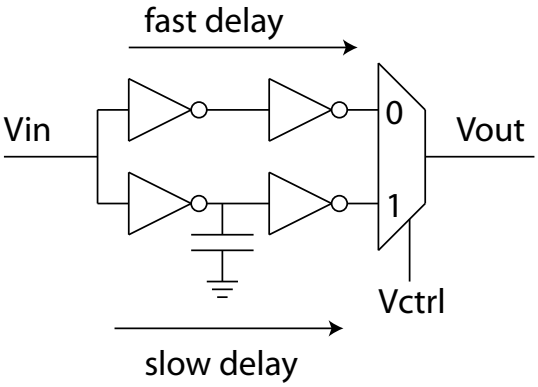

Figure 30: VCDL stage for small delay differences.

The delay stages in the VCDL are different than the oscillator stages. This result in the delay for the VCDL stages changing differently than the delay for the oscillator stages across different PVT conditions. Since the VCDL stages are designed to provide a delay that is an specific fraction of the oscillator period, shifts in the delay for each stage will reintroduce skew between the lines at the receiver after programming. This effect would be minimized by using VCDL delay stages identical to the oscillator stages.

3.2.5 System Simulation

The system has been designed and simulated using a standard 0.25 μm single-poly, five-layer metal CMOS process. PCB traces were simulated using microstrip models and the representative characteristics given in Table 1. The microstrip lines had lengths ranging from 0.5 to 10 inches, corresponding to one way delays from 84 ps to 1.68 ns.

Table 1: Microstrip Line Characteristics

Characteristic	Symbol	Typical Value
Z_0	Characteristic Impedance	50 Ω
C_L	Capacitance per Length	3.36 pF/inch
L_L	Inductance per Length	8.4 nH/inch
v	Propagation Velocity	6×10^9 inch/sec
t_d	Propagation Delay	168 ps/inch

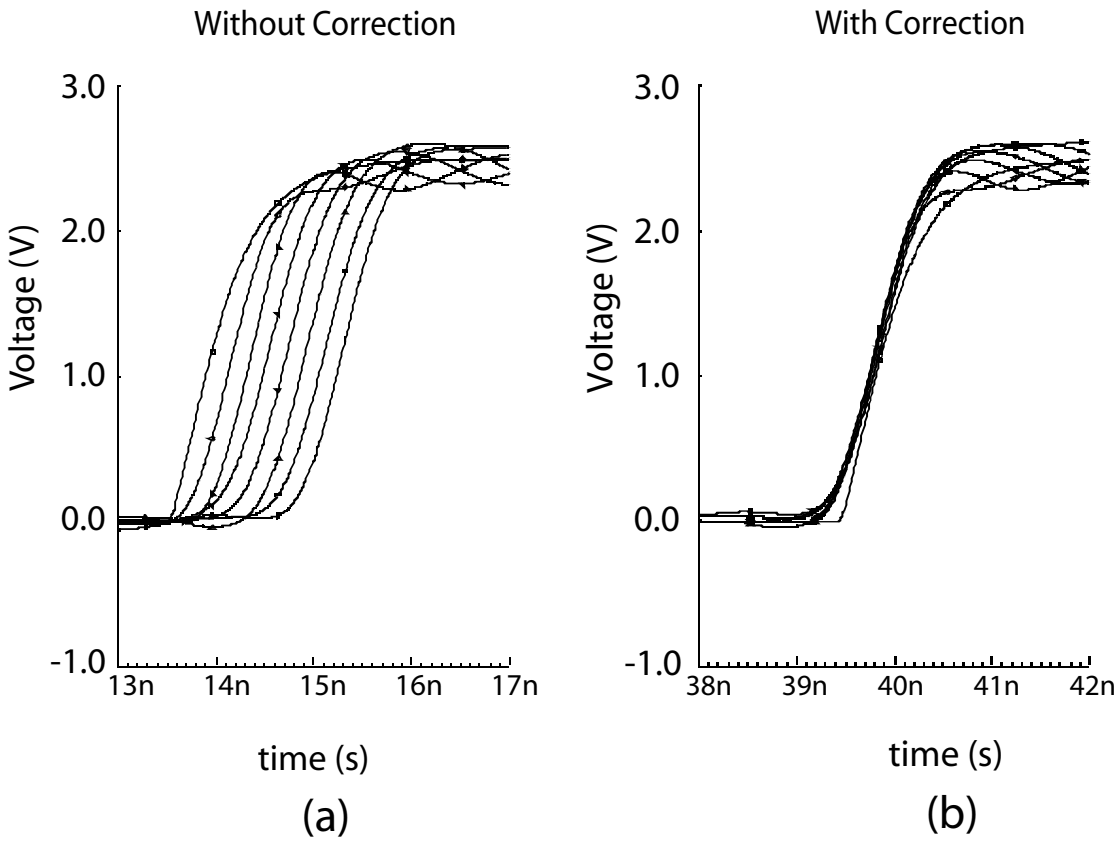

Figure 31: Simulation results of the deskew system for eight lines.

In addition, package capacitance and bond wire inductance were also included in simulation using values of 10 pF and 12 nH respectively as worst case estimates. Simulation results, as shown in Figure 31, indicate that total skew between the lines can be reduced from 1.6 ns to less than 90 ps using the technique presented here for a 200 MHz data stream. This simulation was run for a system with eight different length lines. In general, the maximum delay that can be measured depends on the number of bits in the system. Extension to eight bits, for example, would increase the range by a factor of four. Since line lengths are measured against the resolution of 37.5 ps, lines with propagation delays less than 37.5 ps will be corrected as if they had 0 ps delay. Increasing the resolution of the system allows for measurement of shorter lines and more accurate measurement of long lines.

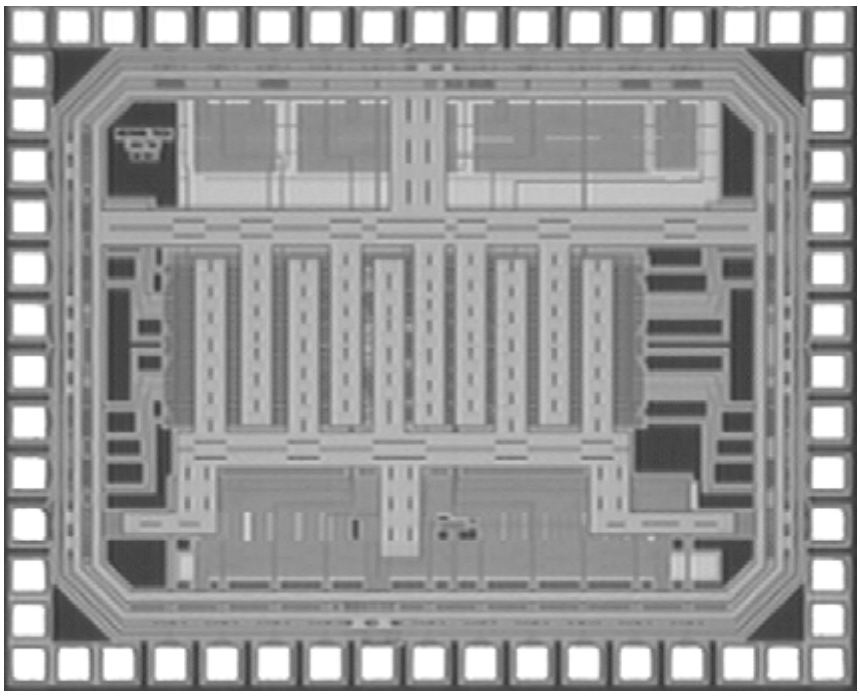

Figure 32: Die photo of the single-ended deskewing chip.

3.3 Characterization and Analysis

For full characterization, the open-loop system described was fabricated in a TSMC 0.25 μm single-poly, five-layer metal CMOS process. A die photo of the entire chip, including the pads, is shown in Figure 32. The total layout area of the core circuitry for an eight line system is 340 μm $\times$ 940 μm.

The peak power dissipation of the system is around 900 mW from a 2.5 V supply for the eight-line system. This is the peak power consumed when the system is being programmed. After programming, the peak power dissipation drops to 250 mW. In general, the power consumed after programming includes only the VCDL and the output driver. Since any system will use an output driver, the additional power consumed by the deskewing system as compared to a system that does not include deskew capabilities is equal to the power consumed only by the VCDL.

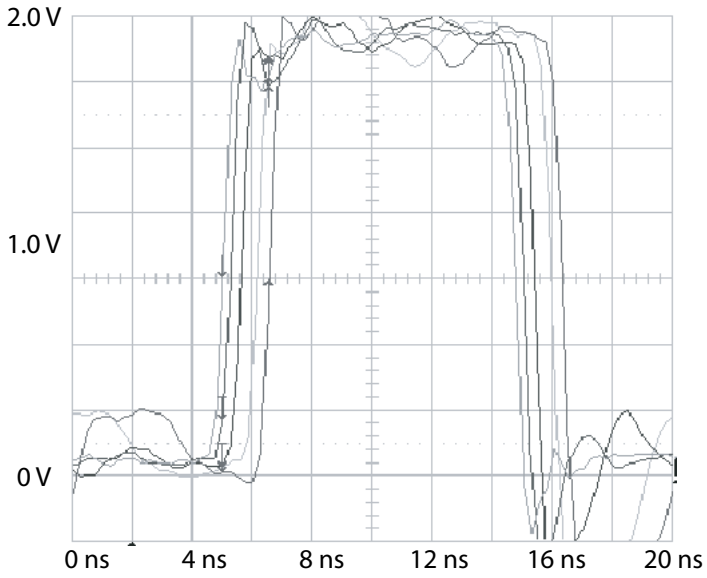

Figure 33: Measured waveforms at the receiver before programming.

3.3.1 Resolution

For measurement of the chip, a custom PCB was manufactured. This test board had eight lines of different lengths, including 0.5, 1.5, 2.5, 3.4, 4.5, 4.5, 8.5, and 10.2 inches. The physical dimensions of the lines are shown in Table 2.

Table 2: PCB Trace Dimensions

Dimension	Value
Width	12.8 mils
Cu Metallization Thickness	1.34 mils
FR-4 Dielectric Thickness	8 mils
FR-4 Dielectric Constant	4.5

Measured signal waveforms at the receiver when all eight lines are pulsed simultaneously are shown in Figure 33. As expected, the difference in line lengths creates a skew at the receiver of over 1.6 ns. The measured waveforms at the receiver after programming are shown in Figure 34. After the deskewing is applied, the signal skew is reduced to less than 90 ps. Only five of the waveforms are shown in the figures because of measurement instrument limitations. The results for the remaining lines

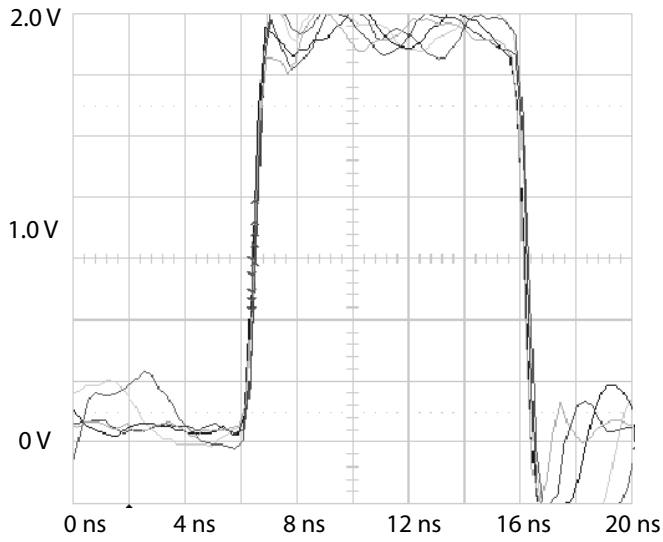

Figure 34: Measured waveforms at the receiver after programming.

are consistent with the displayed waveforms.

3.3.2 Full Scale Range

The full scale range of this system will be limited by two factors - the measurement range and the correction range. The measurement range is set by the number of bits of the counters and the measurement resolution, as given by Equation 14. Increases in the measurement range can be achieved by simply increasing the width of the counters.

The second range limitation is the correction range. This will be set by the VCDL. For a digital VCDL with a quantization factor of t_{min} and N control bits, the maximum correctible range will be

$$T_{correction,max} = t_{min} \times (2^N - 1) \tag{16}$$

Increases to the correctable range can be achieved by adding additional higher-order magnitude blocks to the VCDL. This does not impact the resolution of the VCDL. In general, t_{min} will depend on the process used for fabrication and the oscillator design used, while N will be chosen by the designer to meet the range requirements of the system.

3.3.3 Conversion Time

One possible interpretation of the functionality of this open-loop deskewing system is as a time-to-voltage-to-time converter. The delay measurements process converts the round-trip delay through the PCB traces (a time quantity) into a control word (a voltage quantity). The VCDL then converts the control word (a voltage quantity) back into the appropriate delay (a time quantity). The conversion time is the time required for this process to be completed and is analogous to the programming time of the system. The conversion time will be given by

$$T_{conversion} = T_{offset,VCDL} + T_{buf} + 2t_d + T_{detect} + T_{sum} + T_{compare} + T_{subtract} \quad (17)$$

where $T_{offset,VCDL}$ is the offset delay of the VCDL,T_{buf} is the delay through the output driver, t_d is the one-way delay through the PCB trace, T_{detect} is the delay through the reflection detector, T_{sum} is the time required to calculate the summation of all the counter values, $T_{compare}$ is the time required to determine the maximum of the line delays, and $T_{subtract}$ is the time required to calculate the delay correction for each line. The breakdown of these voltages for the system implemented in a 0.25μm, 2.5 V V_{dd} process are shown in Table 3 for typical process conditions at room temperature.

Table 3: Conversion time breakdown for typical process conditions at room temperature.

Component	Delay
$T_{offset,VCDL}$	2 ns
T_{buf}	300 ps
t_d	1.6 ns
T_{detect}	300 ps
T_{sum}	2.8 ns
$T_{compare}$	3.7 ns
$T_{subtract}$	700 ps
$T_{conversion}$	13 ns

It can be seen from the table that the total programming time will be approximately 13 ns, including a 1.6 ns worst case estimate for the one-way propagation delay through a 10 inch PCB trace. Besides this delay, the conversion time is dominated by the offset delay of the VCDL, the time to calculate the total delay, and the time to determine the maximum delay. In this implementation, both T_{sum} and $T_{compare}$ include the delay through several ripple-carry adders, which dramatically increase the total computation time. Ultimately, however, the system can be programmed in a single pulse (or 13 ns for this implementation). A deskewing system based on a DLL would require many cycles to achieve a final solution. Even though the program time for each cycle in a DLL may be small, the total time will many times that of the cycle time.

3.3.4 Delay

The delay through the deskewing system will limit the maximum operating frequency and play a role in determining suitability of the deskewing system to a particular application. By examination of the Figure 20, it can be seen that the delay through the deskewing system during normal operation will be equal to

$$T_{delay} = T_{offset,VCDL} + T_{program,VCDL} + T_{buf} \tag{18}$$

and includes the offset delay of the VCDL, the delay of the output buffer, and the additional delay programmed into the VCDL ($T_{program,VCDL}$). The first two terms will be determined by the particular technique used for implementation of the VCDL. The third term will depend on the output buffer design. The minimum and maximum delays through the system are shown in Figure 35 and tabulated numerically in Table 4. The minimum delay is when the VCDL control word equals 000000. The maximum delays is when the VCDL control word equals 111111.

In the Figure 35 and Table 4, *Rise Delay* refers to the time between the midpoint on the input rising edge to the midpoint on the output rising edge. *Fall Delay* refers

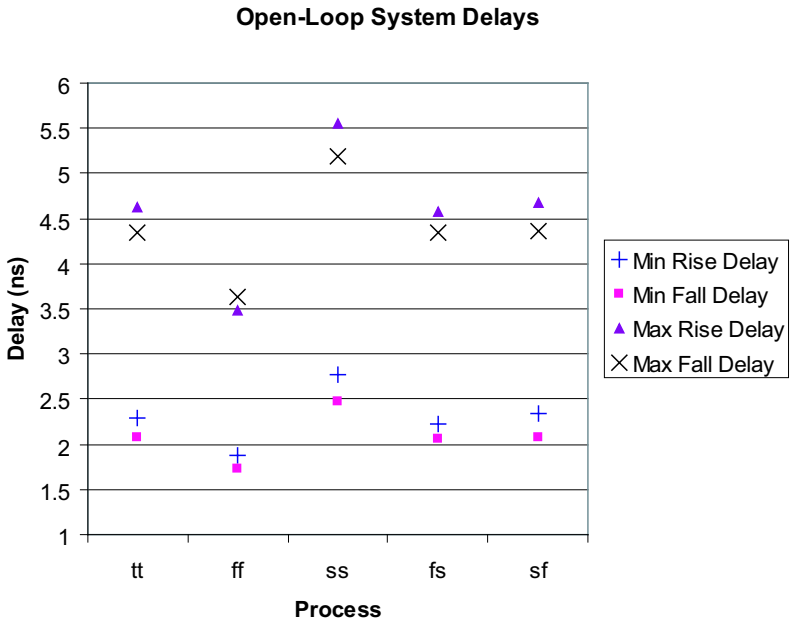

Figure 35: Simulated delays through the open-loop deskewing system for minimum (000000) and maximum (111111) values programmed into the VCDL.

Table 4: Open Loop System Delays

	Min Delay		Max Delay	
Process	Rise Delay (ns)	Fall Delay (ns)	Rise Delay (ns)	Fall Delay (ns)
tt	2.284	2.069	4.626	4.347
ff	1.885	1.730	3.486	3.632
ss	2.766	2.466	5.560	5.188
fs	2.224	2.061	4.580	4.338
sf	2.346	2.080	4.677	4.363

to the time between the midpoint on the input falling edge to the midpoint on the output falling edge.

From Equation 18, the total delay of the system is simply the sum of the VCDL delay and the output buffer delay. Since any application will require an output buffer, the additional delay due to the deskewing system is only the delay of the VCDL.

3.3.5 Maximum Data Rate

The maximum data rate of the open-loop deskewing system is found in simulation and verified experimentally. Using the slowest process parameters, the system is found to be able to support a data rate of 300 MHz for an input signal with a 20% duty cycle. The data rate is limited primarily by the VCDL, which is the dominant block in the signal data path. Using an input with a 50% duty cycle, the maximum frequency is found experimentally to increase to 500 MHz.

3.3.6 Duty Cycle Distortion

In general, the rising and falling edge rates from a particular digital logic gate will be different. This difference arises from differences between the electron and hole mobilities. While a particular gate can be designed to have equal rise and fall time, this will hold only at the particular voltage, temperature, and process conditions used during design. Variations in any of these factors can reintroduce the edge rate variations. In practice, a direct result of this difference in edge rates is a variation in the duty cycle of pulses propagating through the gate. As each edge of the pulse (the rising edge and the falling edge) pass through the gate, they each experience a different delay. The difference in delays reduces the amount of time the signal is high or low, depending on which edge propagates faster. The percent of duty cycle distortion will depend on both the difference in delays and the total period of the signal. As a worst case estimate, a 300 MHz data rate is used for testing.

Simulation results of the duty cycle distortion for the open-loop deskewing system are shown in Figure 36. For this simulation, a data rate of 300 MHz was passed through the system with exactly 20% input duty cycle. The output duty cycle for several process corners for $V_{dd} = 2.5$ V and a temperature of 27 °C are shown. As evident in the figure, the output duty cycle is usually reduced by 4% to 11%. This duty cycle variation occurs primarily in the VCDL. In particular, this VCDL uses passive

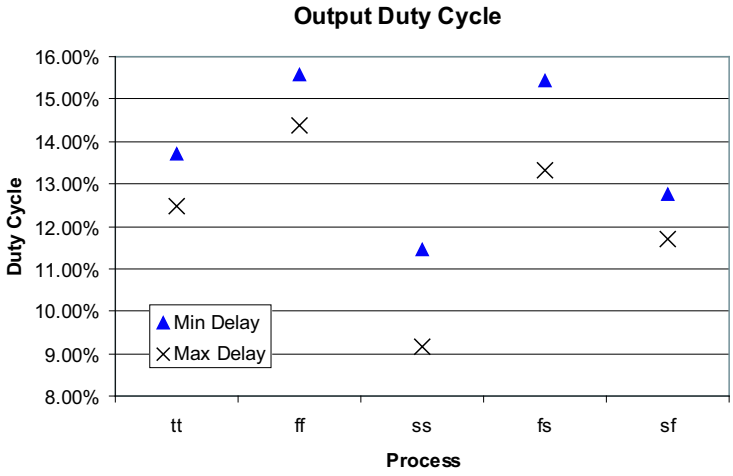

Figure 36: Simulated duty cycle at the output of the open-loop deskewing system for minimum (000000) and maximum (111111) values programmed into the VCDL when the input duty cycle is 50%.

transmission gate multiplexors to control signal flow. The equivalent resistance of these gates exhibits a strong susceptibility to process variation and the delay through these multiplexors is strongly dependant on the drive strength of the preceding gate. In addition, no specific steps were taken to reduce duty cycle distortion. There exist several techniques to minimize the impact of duty cycle distortion which could be applied if necessary in a particular application. Several of these techniques are discussed in Section 5.2.3.

3.3.7 Noise Margin

The noise margins of a system indicate how susceptible the system is to false switching. For the open-loop deskewing system described here, noise is primarily a concern at the output node. This node is the output of the line drivers and the input of the reflection detectors. Specifically, the reflection detectors must be able to sense the reflected pulses. Any false switching of the detectors will introduce errors into the delay correction calculation for the corresponding line. The noise margins of the detector are illustrated in Figure 37. In the figure, V_{IH} represents the input high

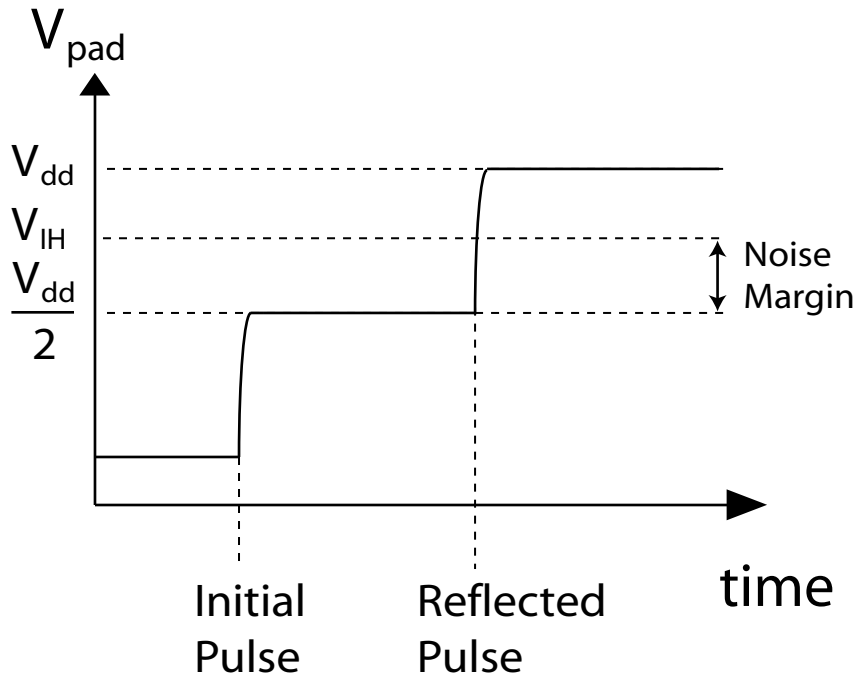

Figure 37: Illustration of reflection detector noise margins.

voltage or trip point for the detector. In addition, it is assumed that the output driver and PCB trace have perfectly matched impedances. To detect the reflections, V_{IH} may be set to the midpoint of the reflected waveform. For a perfectly matched driver and load without a resistive termination, V_{IH} be given by

$$V_{IH} = \frac{V_{dd}}{2} + \frac{V_{dd} - V_{dd}/2}{2} = \frac{3V_{dd}}{4} \tag{19}$$

The noise margin, V_{NM}, is defined as

$$V_{NM} = V_{IH} - V_{pulse,initial} \tag{20}$$

where $V_{pulse,initial}$ is the magnitude of the initial pulse and is assumed to be $V_{dd}/2$ for this perfectly matched system. From this, the ideal noise margin is found to be

$$V_{NM} = \frac{3V_{dd}}{4} - \frac{V_{dd}}{2} = \frac{V_{dd}}{4} \tag{21}$$

This result indicates the ideal noise margin of the reflection detectors. This result is process independent and indicates that the system noise margins are directly proportional to V_{dd}. Therefore, the system noise margins will scale down as V_{dd} scales down

in future lower voltage processes.

There are several significant error sources that can reduce this margin. The first is a shift in V_{IH}. In general, V_{IH} will be given by Equation 13 for a standard CMOS Schmitt Trigger circuit. The forward trip point for this voltage will depend on the specific process parameters, voltage, and temperature of operation. In addition, random process variations in the threshold voltages between the devices can also cause this voltage to shift. If V_{IH} shifts down, it will reduce the noise margin of the system, increasing the susceptibility of the system to false switching. The simulated V_{IH} values for several process corners and temperatures are shown in Figure 21. Simulation indicates that process parameters cause a shift of up to 80 mV and temperature causes a shift of up to 40 mV for this 0.25 μm process.

Another significant error source that cuts into the system noise margin is mismatch between the driver and trace impedances. The magnitude of the initial voltage step that is written to the PCB trace will depend on the relative impedances of the driver and trace. If these impedances are not identical, this voltage will not be equal to $V_{dd}/2$. If the mismatch causes an increase in the initial voltage step of ΔV, this will reduce the noise margin by the same amount, as illustrated in Figure 38.

3.4 Overshoot

Another major issue that concerns the functionality of the deskewing system is inductive peaking or overshoot at the output node. Overshoot will occur at the output node of a system with a high edge rate and substantial pad parasitics, and will therefore exist in most high-speed systems. The universality and magnitude of this problem call for an investigation into the impact of overshoot on the deskewing system, as follows.

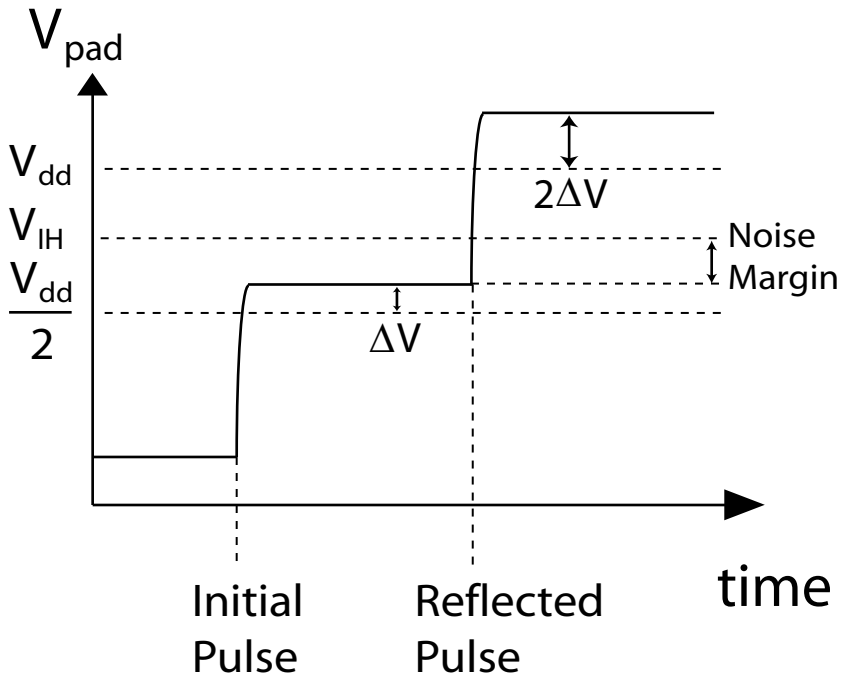

Figure 38: Illustration of reflection detector noise margins.

3.4.1 The Problem With Overshoot

An overshoot event is illustrated on the first rising edge in the waveform in Figure 39. As evident in the figure, the overshoot event on the first rising edge cuts dramatically into the noise margin of the system and can cause false switching of the reflection detectors. After the second rising edge, the detectors will have already switched so overshoot at this point will not pose a problem in this regard and is not discussed here. Overshoot of the sort shown in Figure 39 occurs primarily as a result of pad parasitics - particulary the series inductance. The circuit model used for simulation of these effects is shown in Figure 40. The model is simply a series inductor and a parallel capacitor used to represent the pad parasitics. The parallel capacitor as shown will include the junction capacitance of any electro-static discharge (ESD) structures and the output capacitance of any output drivers.

Overshoot can cause significant problems, particularly for systems with small noise margins. For example, consider the situation in Figure 41. In this example, the

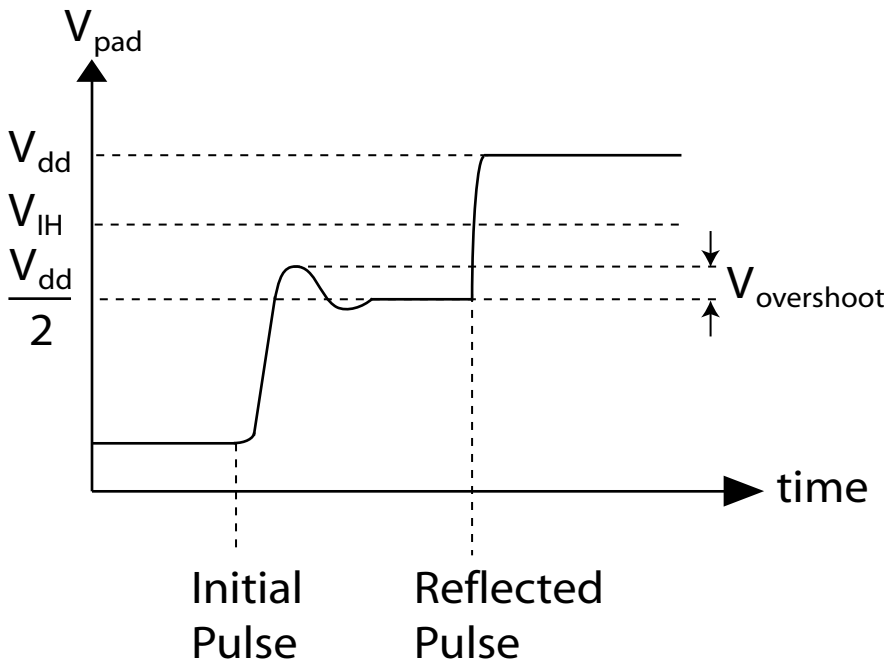

Figure 39: Illustration of overshoot at the output node.

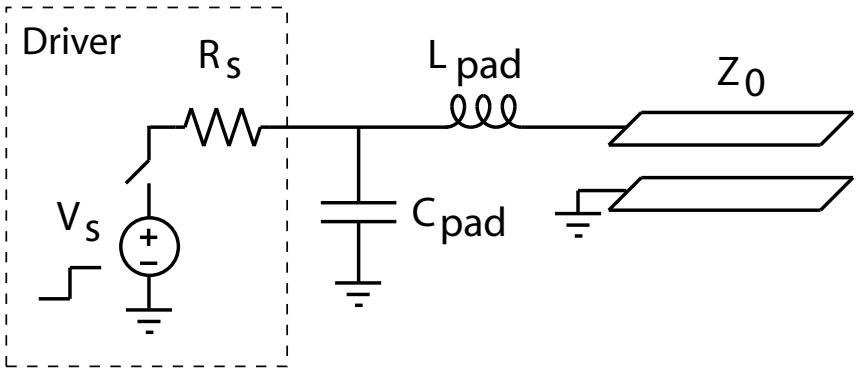

Figure 40: Circuit used to model pad parasitics.

trace impedance is greater than the driver impedance, resulting in an upward shift of V_{mid}. This effect is combined with a downward shift in the V_{IH} of the detector. The downward shift of V_{IH} can be caused by several factors, such as process or temperature variation (as illustrated in Figure 21) or by a drop in V_{dd}. The result of these combined effects is that the peak of the overshoot is now above the V_{IH} level, causing a false switch on every pulse and preventing deskewing of the lines.

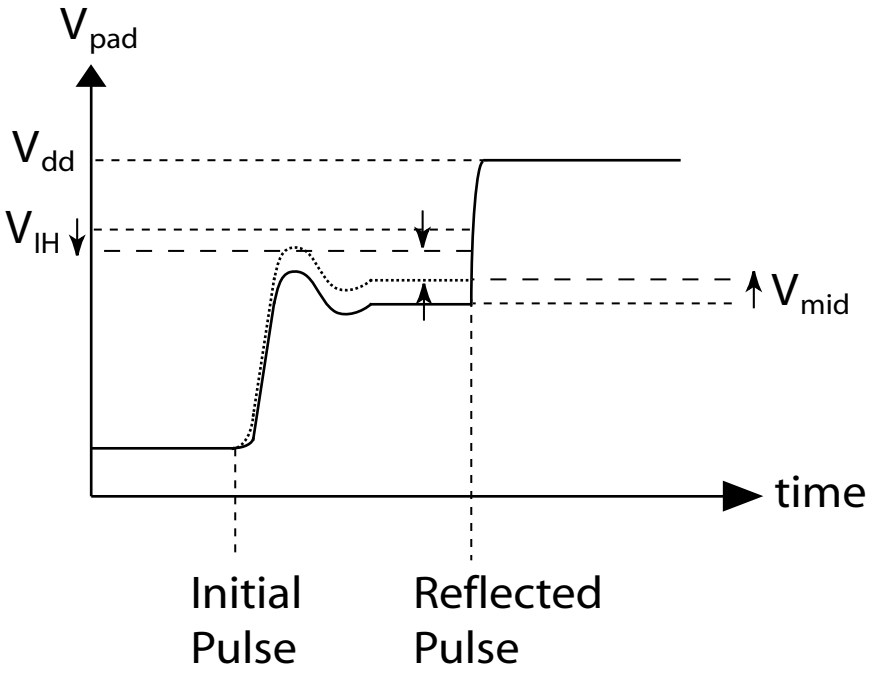

Figure 41: Situation where false switching may occur.

3.4.2 Analysis

For an analysis of the overshoot event, consider the simplified model in Figure 42. This circuit uses an ideal driver, a series inductance (L_{pad}) and parallel capacitance (C_{pad}) to represent the package parasitics, and a resistor ($R_L = Z_0$) to model the PCB trace. If the round trip propagation delay through the line is longer than the overshoot event, then the trace will sink a current inversely proportional to its characteristic impedance. This behavior will be independent of the line termination. In this case, using a simple resistor model is a fair approximation for the PCB trace. The voltage source is a ramp function, as shown in Figure 43(a), which ramps from 0 V at $t = 0$ to V_1 at $t = t_r$ and therefore has a slope of V_1/t_r. This waveform is created from the superposition of two ramp functions (Figure 43(b)), one with slope $+V_1/t_r$ that begins at $t = 0$ and one with slope $-V_1/t_r$ that begins at $t = t_r$. Therefore, the equation for the voltage source will be

$$v_s(t) = \frac{V_1 t}{t_r} u(t) - \frac{V_1(t - t_r)}{t_r} u(t - t_r) \tag{22}$$

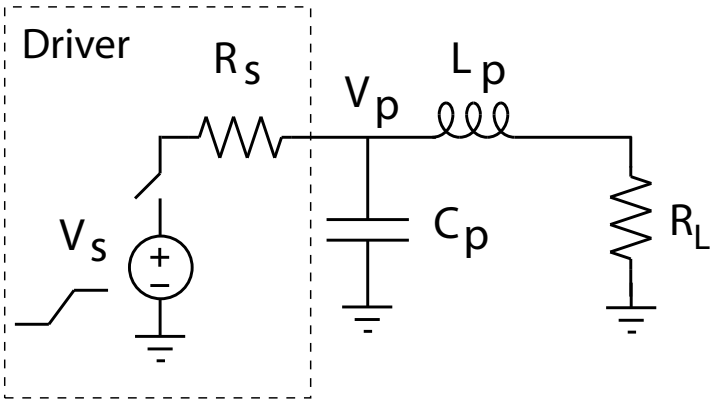

Figure 42: Circuit model used for overshoot analysis.

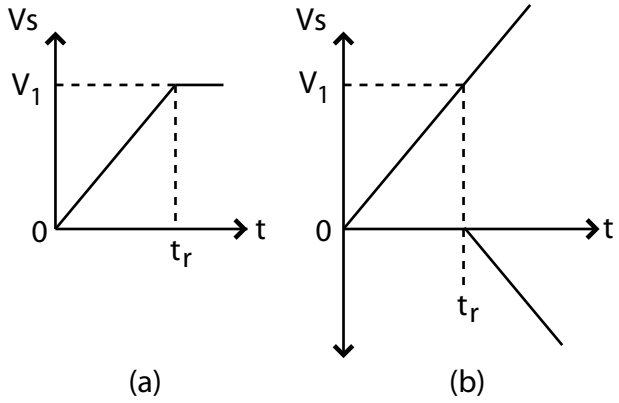

Figure 43: Circuit model used for overshoot analysis.

The Laplace Transform of Equation 22 gives

$$V_s(s) = \frac{V_1}{t_r}\frac{1}{s^2} - \frac{V_1}{t_r}\frac{e^{-t_r s}}{s^2} = \frac{V_1}{t_r}\frac{1}{s^2}(1 - e^{-t_r s}) \tag{23}$$

The voltage at the pad, V_p will be given by

$$V_p(s) = V_s(s)\frac{(sL_p + R_L)//(1/sC_p)}{R_s + (sL_p + R_L)//(1/sC_p)} \tag{24}$$

If it is assumed that $R_s = R_L$, then this equation can be reduced to

$$V_p(s) = \frac{V_1}{t_r}\frac{(sL_p + R_L)(1 - e^{-st_r})}{s^2(2R_L) + s^3(L_p + R_L^2 C_p) + s^4(R_L L_p C_p)} \tag{25}$$

The numerator of Equation 25 is seen to be the difference of two terms, $(1 - e^{-st_r})$. The first term is simply 1. The second term is scaled by e^{-st_r}. Therefore, the inverse

Laplace of $V_p(s)$ will be composed of two portions. The second portion will be identical to the first, but opposite sign and time shifted by t_r.

Equation 25 can be separated into partial fractions. The partial fraction expansion will yield two portions that are identical, except for the scale factor of $-e^{-st_r}$ and will therefore be of the form

$$V_p(s) = V_{p0}(s)\frac{V_1}{t_r}(1 - e^{-st_r}) \tag{26}$$

A partial fraction expansion gives $V_{p0}(s)$ as

$$V_{p0}(s) = \frac{1}{4}\frac{L_P - R_s^2 C_P}{R_s}\frac{1}{s} + \frac{1}{2}\frac{1}{s^2} - \frac{1}{4R_s}\frac{2R_s^2 L_p C_p + L_p^2 - R_s^4 C_p^2 + s(R_s L_p^2 C_p - R_s^3 L_p C_p^2)}{2R_s + sL_p + +sR_s^2 C_p + s^2(R_s L_p C_p)} \tag{27}$$

Examination of Equation 27 reveals that the inverse Laplace transform will yield four terms.

$$\frac{A}{s} \leftrightarrow Au(t) \tag{28}$$

$$\frac{B}{s^2} \leftrightarrow B\,t\,u(t) \tag{29}$$

$$\frac{C_1(s+a)}{(s+a)^2 + w^2} \leftrightarrow C_1\,e^{-at}cos(\omega t) \tag{30}$$

$$\frac{C_2\,\omega}{(s+a)^2 + \omega^2} \leftrightarrow C_2\,e^{-at}sin(\omega t) \tag{31}$$

where C_1, C_2, a, and ω are constant coefficients that will be determined. Several of the coefficients are apparent from direct observation, as follows.

$$A = \frac{1}{4}\frac{L_p - R_s^2 C_p}{R_s} \tag{32}$$

$$B = \frac{1}{2} \tag{33}$$

The remaining unknowns, C_1, C_2, a and ω must be calculated. The calculation is shown in Appendix A. The results are summarized below.

$$a = \frac{1}{2}\Big(\frac{1}{R_s C_p} + \frac{R_s}{L_p}\Big) \tag{34}$$

$$\omega = \frac{1}{2}\sqrt{\frac{6}{L_p C_p} - \frac{1}{R_s^2 C_p^2} - \frac{R_s^2}{L_p^2}} \tag{35}$$

$$C_1 = \frac{1}{4}\left(R_s C_p - \frac{L_p}{R_s}\right) \tag{36}$$

$$C_2 = \frac{1}{8\omega}\left(\frac{R_s}{L_p} R_s C_p - \frac{L_p}{R_s}\frac{1}{R_s C_p} - 4\right) \tag{37}$$

Therefore, the final voltage will be given by

$$\begin{aligned} V_p(t) = {} & \tfrac{V_{dd}}{t_r}\Big[A + Bt + C_1 e^{-at} cos(\omega t) + C_2 e^{-at} sin(\omega t)\Big] - \\ & \tfrac{V_{dd}}{t_r}\Big[A + B(t - t_r) + C_1 e^{-a(t-t_r)} cos(\omega(t - t_r)) + C_2 e^{-at} sin(\omega(t - t_r))\Big] u(t - t_r) \end{aligned} \tag{38}$$

One simple observation can immediately be seen from Equation 38. The magnitude of the output waveform and therefore the magnitude of the overshoot will depend directly on the magnitude of V_{dd}. The amount of overshoot as a percentage of the power supply will therefore be a constant when all other factors remain constant. To gather any more intuition from this result, another assumption must be made. It is assumed that the ratio of L_p to C_p is a constant and, furthermore, that this constant will be given by

$$\frac{L_p}{C_p} = R_s^2 \tag{39}$$

which leads to

$$C_p = \frac{L_p}{R_s^2} \tag{40}$$

Note that

$$R_s C_p = \frac{L_p}{R_s} \tag{41}$$

Of the assumptions made so far, this is the most egregious, as the ratio of L_p to C_p will depend on the package used and may not have the specific value expected. However, typical values of $L_p = 7.5\,nH$, $C_p = 3\,pF$, and $R_s = 50\,\Omega$ meet this condition. Therefore, the results should be relevant to an actual system whose characteristics do not deviate too greatly from the typical values.

Substituting Equation 39 into the equations for the coefficients derived earlier gives simplified results, as shown.

$$A = 0 \tag{42}$$

$$B = \frac{1}{2} \tag{43}$$

$$a = \frac{R_s}{L_p} \tag{44}$$

$$\omega = \frac{1}{2}\sqrt{6\frac{R_s^2}{L_p^2} - \frac{R_s^2}{L_p^2} - \frac{R_s^2}{L_p^2}} = \frac{R_s}{L_p} \tag{45}$$

$$C_1 = 0 \tag{46}$$

$$C_2 = \frac{1}{8}\frac{L_p}{R_s}(1 - 1 - 4) = -\frac{1}{2}\frac{L_p}{R_s} \tag{47}$$

Substituting these simplified expressions into Equation 38 gives

$$\begin{aligned} V_p(t) = \tfrac{V_{dd}}{t_r}\Big[Bt + C_2 e^{-at} sin(\omega t)\Big] - \\ \tfrac{V_{dd}}{t_r}\Big[B(t - t_r) + C_2 e^{-at} sin(\omega(t - t_r))\Big] u(t - t_r) \end{aligned} \tag{48}$$

To determine the magnitude of the peaking, it must first be determined the time that the peak voltage occurs, t_{peak}. Examination of the terms in Equation 48 lead to some observations. First, the terms Bt and $B(t - t_r)$ will cancel to give a constant at times $t > t_r$. Therefore, the peaking will result from the sum of the remaining two terms. These terms are plotted in Figure 44. The second term, $p2 = C_2 e^{-at} sin(\omega(t - t_r))u(t - t_r)$, is simply a time-shifted version of the first term, $p1 = C_2 e^{-at} sin(\omega t)$.

To be useful, the final result for the overshoot voltage must be sufficiently simple that some intuition can be derived from the equation. Therefore, one more simplifying assumption will be required. It will be assumed here that $(p1 - p2)$ peaks when $sin(\omega(t - t_r))$ is a maximum. In general, the peak of $(p1 - p2)$ will occur before the peak of $sin(\omega(t - t_r))$, as can be seen in Figure 44. However, this is the closest approximation that yields useful results. The peak of a *sin* function occurs when the argument is equal to $\pi/2$. Therefore,

$$\omega(t_{peak} - t_r) = \pi/2 \tag{49}$$

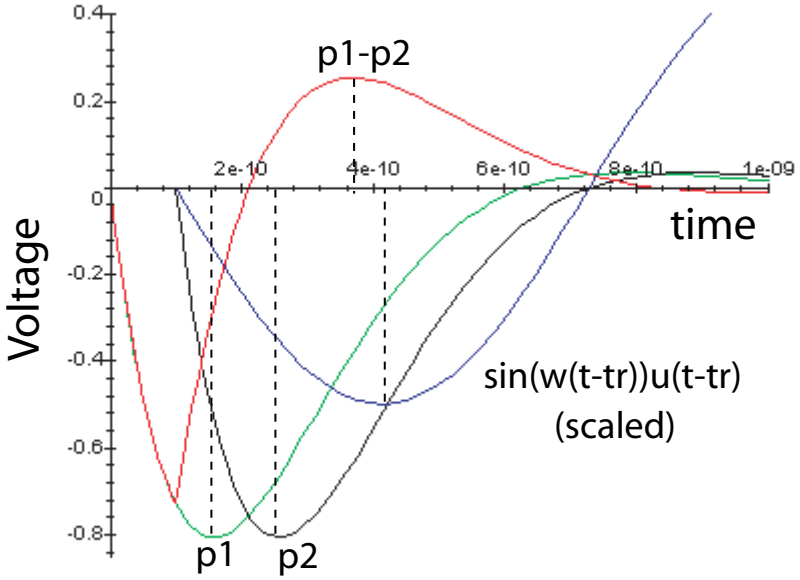

Figure 44: Plots of some terms that contribute to overshoot. The sin function has been scaled to fit on the same axis.

This can be solved for t_{peak} to give

$$t_{peak} = \frac{\pi}{2\omega} + t_r \tag{50}$$

Substituting Equation 45 into Equation 50 gives

$$t_{peak} = \frac{\pi}{2}\frac{L_p}{R_s} + t_r \tag{51}$$

Substitution of Equation 51 into Equation 48 gives

$$V_p(t_{peak}) = \frac{V_{dd}}{t_r}\left[\frac{1}{2}t_r - \frac{1}{2}\frac{L_p}{R_s}e^{-\frac{R_s}{L_p}\frac{\pi}{2}\frac{L_p}{R_s}}e^{-\frac{R_s}{L_p}t_r}sin(\frac{R_s}{L_p}\frac{\pi}{2}\frac{L_p}{R_s} + \frac{R_s}{L_p}t_r) + \frac{1}{2}\frac{L_p}{R_s}e^{-\frac{R_s}{L_p}\frac{\pi}{2}\frac{L_p}{R_s}}sin(\frac{R_s}{L_p}\frac{\pi}{2}\frac{L_p}{R_s})\right] \tag{52}$$

which can be reduced to

$$V_p(t_{peak}) = \frac{V_{dd}}{t_r}\left[\frac{t_r}{2} - \frac{1}{2}\frac{L_p}{R_s}e^{-\frac{\pi}{2}}e^{-\frac{R_s}{L_p}t_r}sin(\frac{\pi}{2} + \frac{R_s}{L_p}t_r) + \frac{1}{2}\frac{L_p}{R_s}e^{-\frac{\pi}{2}}\right] \tag{53}$$

and further simplified to

$$V_p(t_{peak}) = \frac{V_{dd}}{t_r}\left[\frac{t_r}{2} + \frac{1}{2}\frac{L_p}{R_s}e^{-\frac{\pi}{2}}\left(1 - e^{-\frac{R_s}{L_p}t_r}cos(\frac{R_s}{L_p}t_r)\right)\right] \tag{54}$$

This simplified equation will predict the peak value of the overshoot as a function of the parasitic inductance and driver impedance, given that the previous assumptions hold. It is important to note at this point that the peak voltage is directly proportional to V_{dd} and inversely proportional to t_r. Therefore, signals with smaller rise times (and faster edge rates) will experience a greater degree of overshoot. The assumptions made in the derivation are listed below.

1. The circuit in Figure 42 adequately represents the effects of package parasitic inductance (L_p) and capacitance (C_p).

2. The driver and trace impedances are matched ($R_s = R_L$).

3. The PCB trace is sufficiently long that it can be modelled as a resistor. This will be the case when the round-trip propagation delay through the line exceeds the duration of the peaking event.

4. L_p/C_p is a fixed ratio and equal to R_s^2

5. Peaking occurs at the maximum of the $sin(\omega(t - t_r))$ function.

Examination of Equation 54 indicates immediately the peak voltage is the sum of two terms. The first term is simply $V_{dd}/2$, which is ideal voltage in the absence of any peaking and will be the steady-state solution before the reflected waveform appears. Therefore, the magnitude of the peaking will be determined primarily by the second term. The behavior of this expression is best illustrated graphically. Figure 45 shows a plot of the total peak voltage (Equation 54) versus L_p when $R_s = 50\,\Omega$ and $t_r = 100\,ps$. As evident in Figure 45, the peak voltage will approach a constant value for large inductance values. To determine this final value, the limit as L approaches infinity must be taken. To do this, a simple substitution is used, as shown below.

$$x = \frac{L_p}{R_s}\frac{1}{t_r} \tag{55}$$

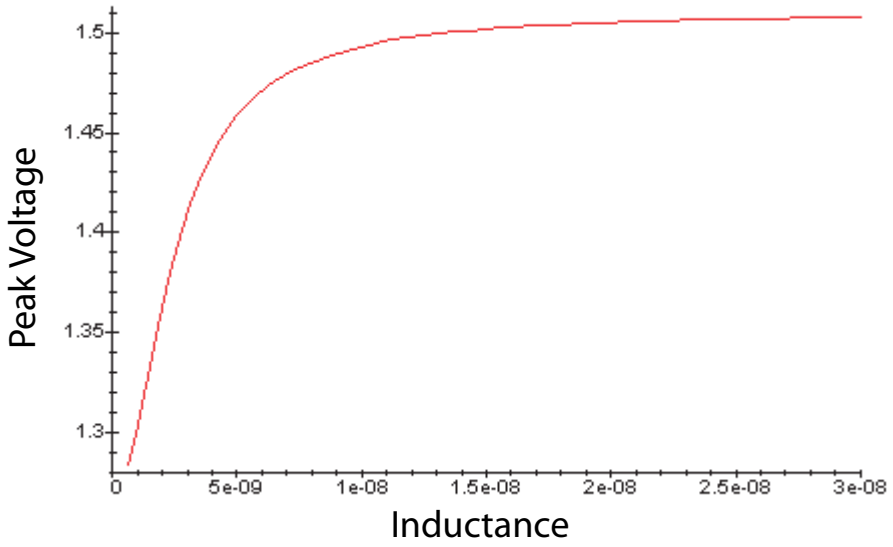

Figure 45: Peak overshoot voltage versus parasitic inductance value.

Equation 54 can then be rewritten as

$$V_{peak} = \frac{V_{dd}}{2} + V_{dd}\frac{e^{-\pi/2}}{2}x\Big(1 - e^{-1/x}cos(1/x)\Big) \tag{56}$$

Then,

$$\lim_{x\to\infty} V_{peak} = \lim_{x\to\infty}\left[\frac{V_{dd}}{2} + V_{dd}\frac{e^{-\pi/2}}{2}x\Big(1 - e^{-1/x}cos(1/x)\Big)\right] \tag{57}$$

which is equal to

$$\frac{V_{dd}}{2} + V_{dd}\frac{e^{-\pi/2}}{2}\lim_{x\to\infty} x\Big(1 - e^{-1/x}cos(1/x)\Big) \tag{58}$$

At this point, L'Hôpital's rule must be used to determine the limit of the right term. Application of L'Hôpital's rule occurs as follows:

$$\lim_{x\to\infty} x\Big(1 - e^{-1/x}cos(1/x)\Big) = \lim_{x\to\infty}\frac{\Big(1 - e^{-1/x}cos(1/x)\Big)}{1/x} \tag{59}$$

$$= \lim_{x\to\infty}\frac{\frac{d}{dx}\Big(1 - e^{-1/x}cos(1/x)\Big)}{\frac{d}{dx}(1/x)} = \lim_{x\to\infty}\frac{\Big(\frac{-e^{-1/x}cos(1/x)}{x^2} - \frac{e^{-1/x}sin(1/x)}{x^2}\Big)}{(-1/x^2)} \tag{60}$$

$$= \lim_{x\to\infty}\Big(e^{-1/x}cos(1/x) + e^{-1/x}sin(1/x)\Big) \tag{61}$$

$$= e^0 cos(0) + e^0 sin(0) = 1 \tag{62}$$

Therefore,

$$\lim_{L_p \to \infty} V_{peak} = \frac{V_{dd}}{2} + V_{dd}\frac{e^{-\pi/2}}{2} = \frac{V_{dd}}{2} + 0.104V_{dd} \tag{63}$$

This result is for a specific case - a fixed ratio of L_p/C_p and a matched driver and load. However, the result is still significant. It indicates that the maximum overshoot is approximately a constant for a given L_p/C_p value, provided that L_p is sufficiently large. The exact value that constitutes "sufficiently large" will depend on the signal rise time and driver impedance.

As a final observation, Figure 46 shows a plot of the overshoot voltage versus t_r when $R_s = 50\,\Omega$ and $L_p = 10\,nH$. As evident in the figure, the characteristic is dominated by the $1/t_r$ behavior for most of the range shown. Based on this observation, a simple rule of thumb is that the overshoot voltage doubles every time the rise time is halved.

3.4.3 Characterization

To verify the analytical model, a characterization of the overshoot event will be performed using simulation. The magnitude of the overshoot will depend on several factors, as discussed previously. One important factor is the edge rate of the first rising edge. Signals with a higher edge rate will experience larger overshoot voltages, as evident in Equation 54. Figure 47 shows simulation results of the the peak voltage of the overshoot as a function of the signal rise time. Signals that have a smaller rise time (and therefore a higher edge rate) experience a greater degree of overshoot. This is a problem in high-speed signal transmission, where the PCB trace rise times are forced to be less than 1 ns for data transmission in the 100's of MHz range. For this simulation, the circuit of Figure 40 is used, where an ideal 50 Ω driver is used to drive a perfectly matched 50 Ω line. The series inductance and parallel capacitance are taken to be 2.5 nH and 1 pF respectively as typical or slightly optimistic values.

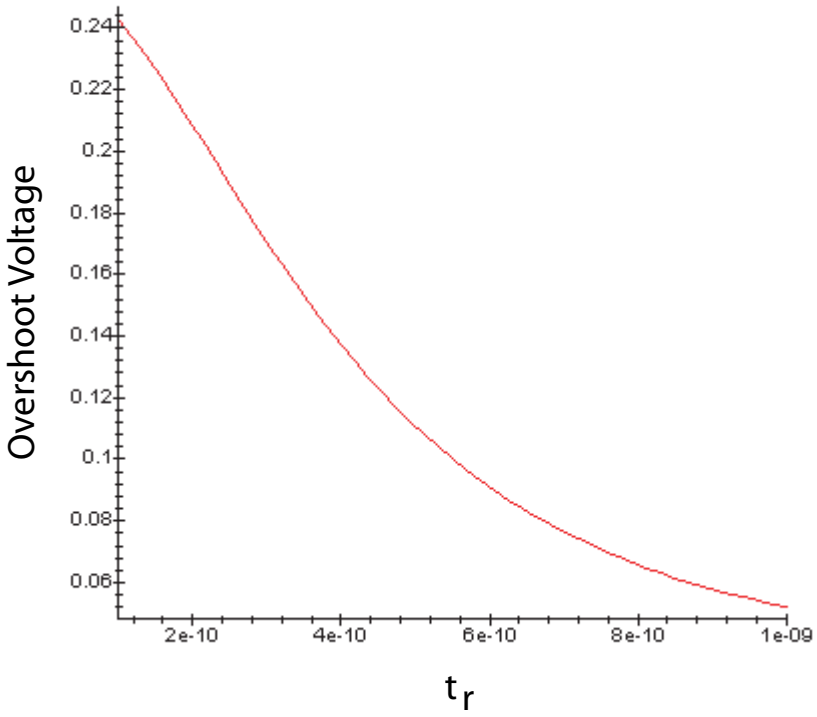

Figure 46: Peak overshoot voltage versus parasitic inductance value.

The peak in the absence of overshoot would be $V_{dd}/2$ or 1.25 V for this simulation. As the signal rise time becomes very large, the magnitude of the peaking decreases.

For the system that has been implemented here in a 0.25 μm, 2.5 V process, overshoot as dramatic as 200 mV or 300 mV is still within the noise margins of the system, as long as the trace and driver impedances are relatively well matched. However, the problem of overshoot becomes much more significant as V_{dd} drops. From Equation 21, it can be seen that the noise margin is a fixed percentage of V_{dd} and will therefore decrease directly with V_{dd}. The problem that then arises is the rate at which overshoot scales with decreasing V_{dd}. This effect is illustrated in Figure 48. The data in the figure is a result of simulations using the ideal circuit in Figure 40 where the driver impedance is perfectly matched to the trace impedance. The overshoot

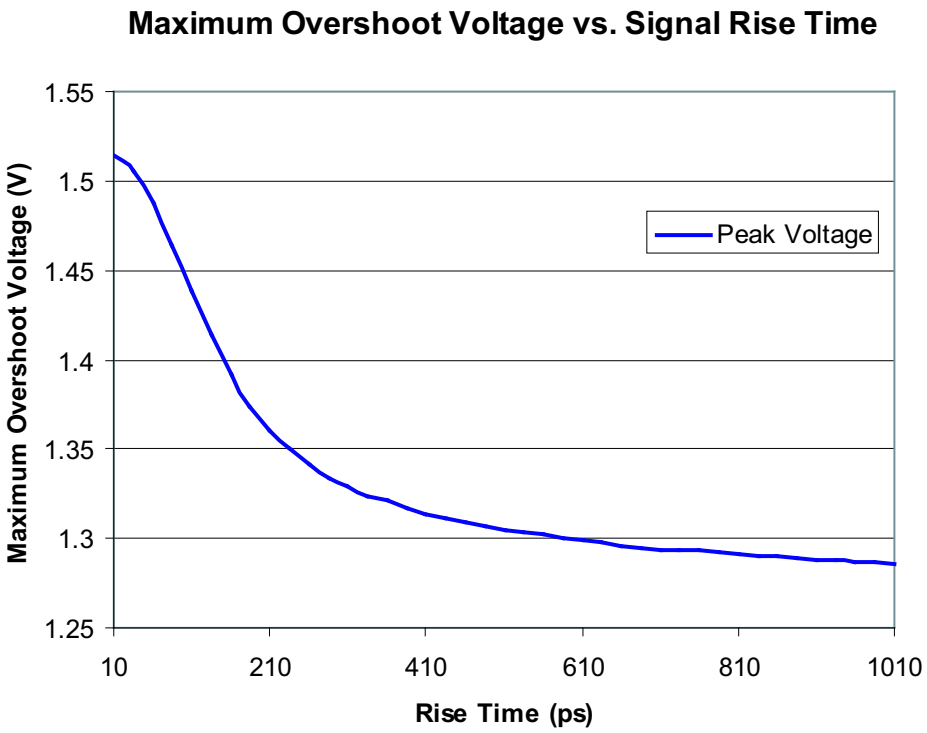

Figure 47: Overshoot voltages for different edge rates.

percentage is defined as

$$Overshoot\,Percentage = \frac{V_{overshoot}}{V_{dd}} \times 100 \tag{64}$$

For the simulations, the signal rise time was held constant at 100 ps as the power supply was varied. The rise time is defined here as the time required for the source voltage to ramp from 0 V to V_{dd}, as shown in Figure 49. For lower supply voltages, the signal has a lower voltage swing during the rise time, resulting in a slower edge rate. As evident in the figure, the overshoot expressed as a percentage of V_{dd} remains constant across V_{dd} from 0 V to 5 V for a constant rise time. This is as expected from Equation 54.

To examine this effect of signal rise times on overshoot, simulation was performed across V_{dd} for a system having a constant edge rate. If the edge rate is constant, then signals with lower voltage swings will also have a lower rise time. The results

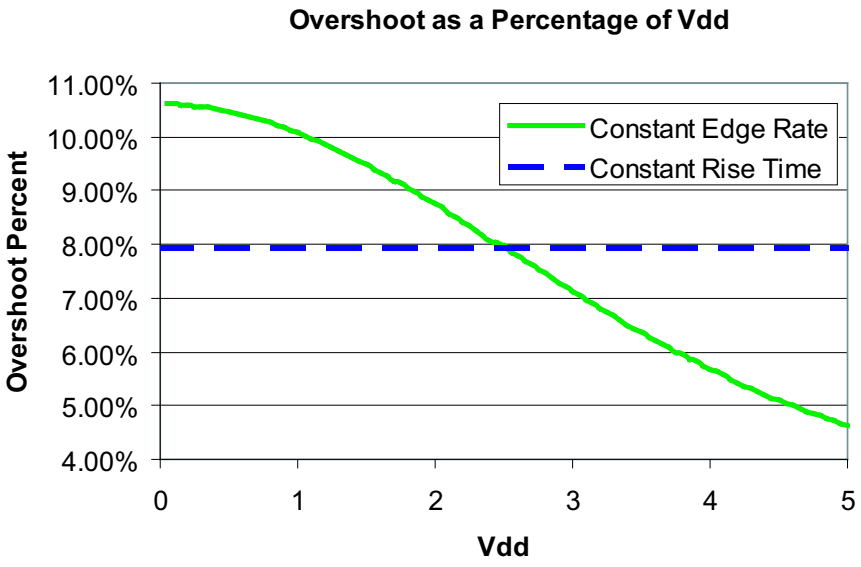

Figure 48: Overshoot as a percentage of V_{dd} for a range of V_{dd} values. Simulations were performed using constant edge rates and constant rise times.

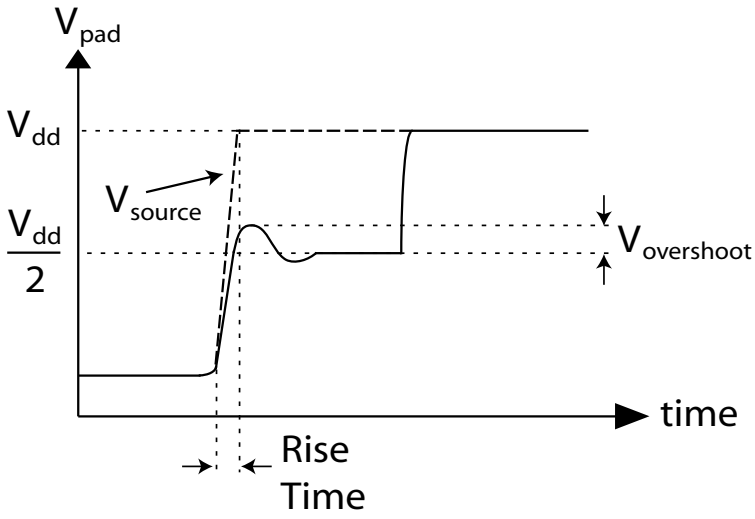

Figure 49: Illustration of the definitions of edge rate and rise times.

of this simulation are also shown in Figure 48. The simulation is set up such that the 2.5 V system has a signal rise time of 100 ps. As can be seen in the figure, for a constant edge rate, the percentage of overshoot increases as V_{dd} decreases. If the edge rate is held constant instead of the rise time, the effect of overshoot becomes much more dramatic at lower supply voltages. Once again, this is in accord with

the analytical result in Equation 54. This presents a potential problem for future systems, which may attempt to drive the external traces at increasing frequencies. The simulations performed were independent of process and included only parasitic package inductance and capacitance. Overshoot will become a limiting factor for using time domain reflectometry in these systems if the pad parasitics are not also scaled down appropriately for low voltage systems.

3.4.4 Extension

If both the overshoot and the noise margins scale in the same manner with V_{dd}, then overshoot would not pose a greater problem for future lower-voltage systems than for the present 2.5 V system. Instead, other noise sources would become limiting factors as the noise margin shrinks. This, however, is based on the assumption that the signal rise time remains constant. In general, it must be considered that a future system may operate at a higher data transmission rate, requiring a decrease in signal rise times. As demonstrated above, decreasing rise times lead to increased overshoot. Decreasing supply voltages lead to decreased system noise margins. The combination of lower power supply voltages and increased signal transmission rates in future systems makes overshoot a critical problem.

3.5 Capacitive Terminations

Another issue that must be considered is the variations introduced by having different load conditions on each of the traces. This situation may easily arise in a real application. For example, if the system is used to send a deskewed clock signal to several different receiver chips, each chip may be packaged differently and have different input circuits. Each different input circuit and package will add a different capacitive loading to the line. The question that arises is how the capacitive loading effects the signals as seen at the transmitting chip. The transmitted pulse depends only on the trace impedance and parasitics of the transmitting chip. Therefore, this waveform

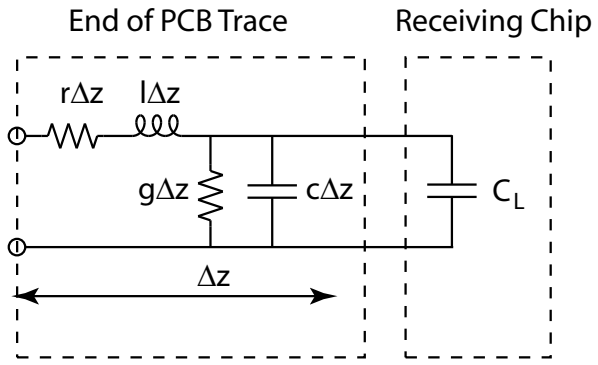

Figure 50: Circuit model at the receiver end of a PCB trace including the last differential line element and the capacitive load.

will be the same for every trace. The differences created by the capacitive loads will, however, directly impact the reflected waveforms. In general, is it desirable to have a simple model than can be used to predict how the deskewing system will behave when each line has a different capacitive termination. This section will develop a simple model for predicting the effects of a range of capacitive loading on the signal waveforms. This model can be used to predict the behavior of the deskewing system in the presence of differently loaded lines.

3.5.1 A Simple Model

A simple model for the effect of a load capacitor can be developed by considering the basic line characteristics. A PCB trace is typically modelled using differential line elements consisting of series inductors and parallel capacitors. The trace will have a characteristic inductance and capacitance per unit length, which will depend on the exact line geometry and board composition. The end of the trace will then be as shown in Figure 50.

In the figure, $r\Delta z$ is the series resistance, $l\Delta z$ is the series inductance, $g\Delta z$ is the parallel conductance, and $g\Delta z$ is the parallel capacitance where all circuit element quantities are expressed per unit length and Δz is the length of the differential line element. Assume that a standard PCB trace has negligible r and g. This leaves only

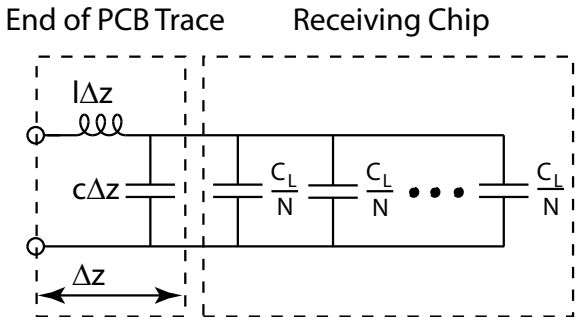

Figure 51: Circuit model at the receiver end of a PCB trace incorporating several assumptions.

the series inductance and parallel capacitance per unit length. Next, the load capacitance is broken into N equal magnitude parallel capacitors, as shown in Figure 51. The factor N is determined by

$$N = \frac{C_L}{c\Delta z} \tag{65}$$

where C_L is the magnitude of the load capacitance. The next interpretation of this circuit incorporates the most egregious assumption - the N segments of the capacitive load are treated as being equivalent to N sections of transmission line of length Δx. The total equivalent length of the N sections will be

$$L_{additional} = N\Delta x = \frac{C_L}{c\Delta z}\Delta z \tag{66}$$

The problem with this simplification is that it neglects the effect of the series inductance on the signal propagation through the line. The consequences of this assumption will be demonstrated below. The final model for considering the effects of load capacitance is as follows: a load capacitor of magnitude C_L behaves as an extension of the PCB trace, adding an additional length of $L_{additional}$, as given by Equation 66. Therefore, the additional skew created by a load capacitor of magnitude C_L will be

$$t_{skew,cap} = t_{pd}L_{additional} = t_{pd}\frac{C_L}{c\Delta z}\Delta x \tag{67}$$

where t_{pd} is the signal propagation delay per unit length and has units of $time/length$. The physical interpretation of this model is straightforward. If the PCB trace is

treated as a large capacitor, then the propagation delay is simply the time required for the driver to discharge the line. For a driver with a constant output impedance, the load capacitance at the end of the line will be discharged at the same rate as the rest of the line (i.e. there is a constant current through the driver). Therefore, the load capacitance provides an additional delay proportional to the magnitude of the load.

3.5.2 Model Verification

Verification of this model was performed through simulation using an ideal driver and a microstrip PCB trace model. The dimensions of the trace are chosen to match those of the board fabricated for testing the open-loop deskewing system and are give in Table 2. Using these physical dimensions gives the capacitance per unit length to be

$$c = 2.791\, pF/inch \tag{68}$$

and the signal propagation delay to be

$$t_{pd} = 141.7\, ps/inch \tag{69}$$

For simulation, the test setup of Figure 52 is used. In this test setup, two lines are tested. One line is terminated with a capacitor of magnitude C_L. The other line is identical to the first, but has an extra length in place of the capacitive load, as given by Equation 66, and no other load termination. The simulated delays from the driver rising edge to the midpoint of the rising edge at the receiver are shown in Figure 53. The delay expected from a capacitive load match closely to the delay created by an additional length of line, especially for smaller loads. The greatest error occurs at very heavy loads ($> 8\ pF$) where the additional length of line (> 2 inches) becomes as substantial fraction of the length of the actual line (6 inches).

The model is seen to be relatively accurate for predicting delay to the receiver. The next question is the impact on the delay needed for the reflected pulse to return

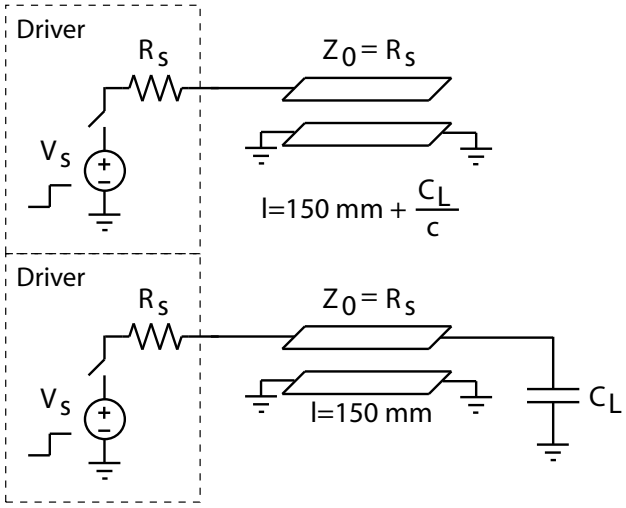

Figure 52: Simulation setup used to test capacitive loading model.

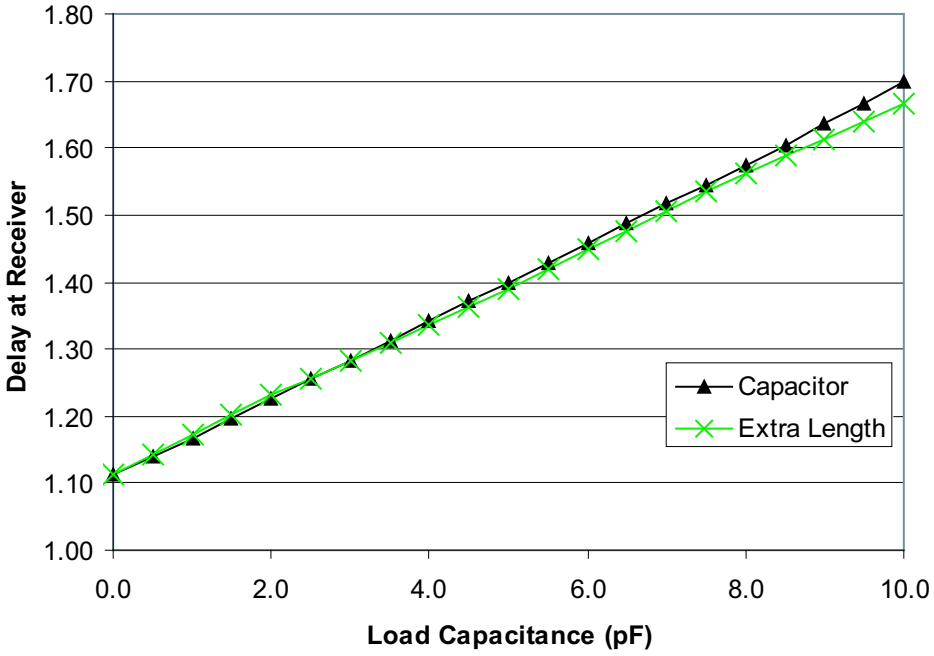

Figure 53: Delays to the receiver for several loads and equivalent lengths.

to the driver. This delay will be the one seen by a deskewing system that relies on time domain reflectometry to measure line lengths. Any error that appears in the reflected waveforms will directly impact deskewing system performance. The

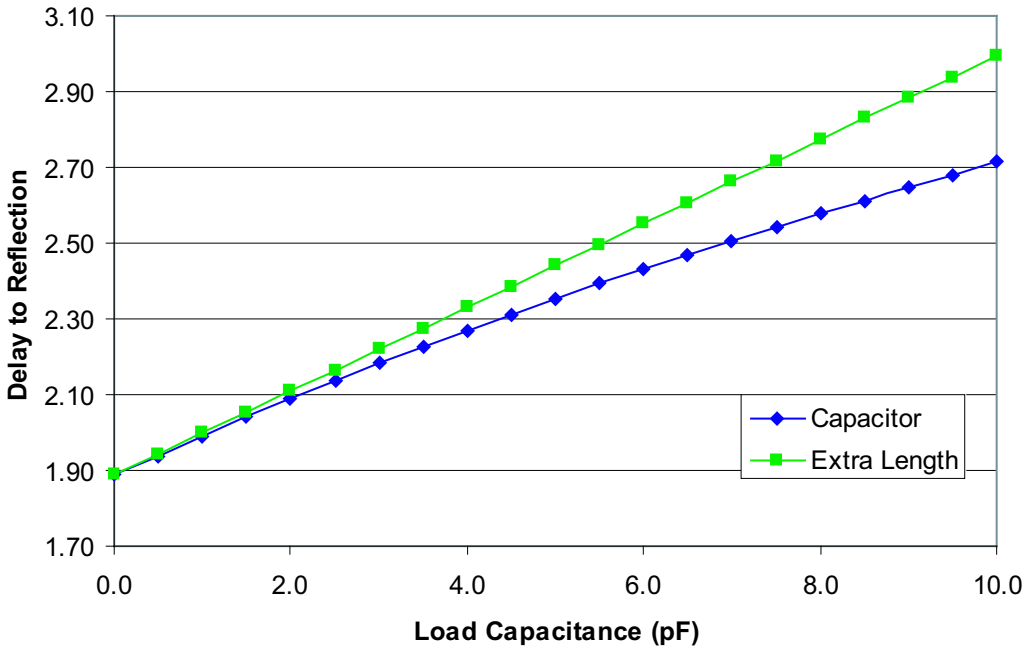

Figure 54: Reflection delays for several loads and equivalent lengths.

simulation results for these delays are shown in Figure 54. The delay for the reflection does not display as great a degree of accuracy as the delay to the receiver. This is due primarily to the assumptions made previously - primarily the absence of a series inductor corresponding to the large load. Since there is no series inductor at the load, the reflection will begin shortly after the forward travelling wave reaches the termination for the capacitively terminated line. The line with the extra length, however, does not provide a reflection until the wave reaches the end of the line. In addition, the large capacitor at the load end of the line initially acts like a short circuit. This results in a dip in the reflected waveform before the reflected voltage rises to V_{dd}. Finally, the capacitive termination decreases the edge rate of the reflected wave. This results in the reflection taking longer to rise to the detector trip point than the reflection from the unterminated line. Therefore, the lines with a capacitive termination will measure a delay larger than that for the unterminated line when measured at the same trip point.

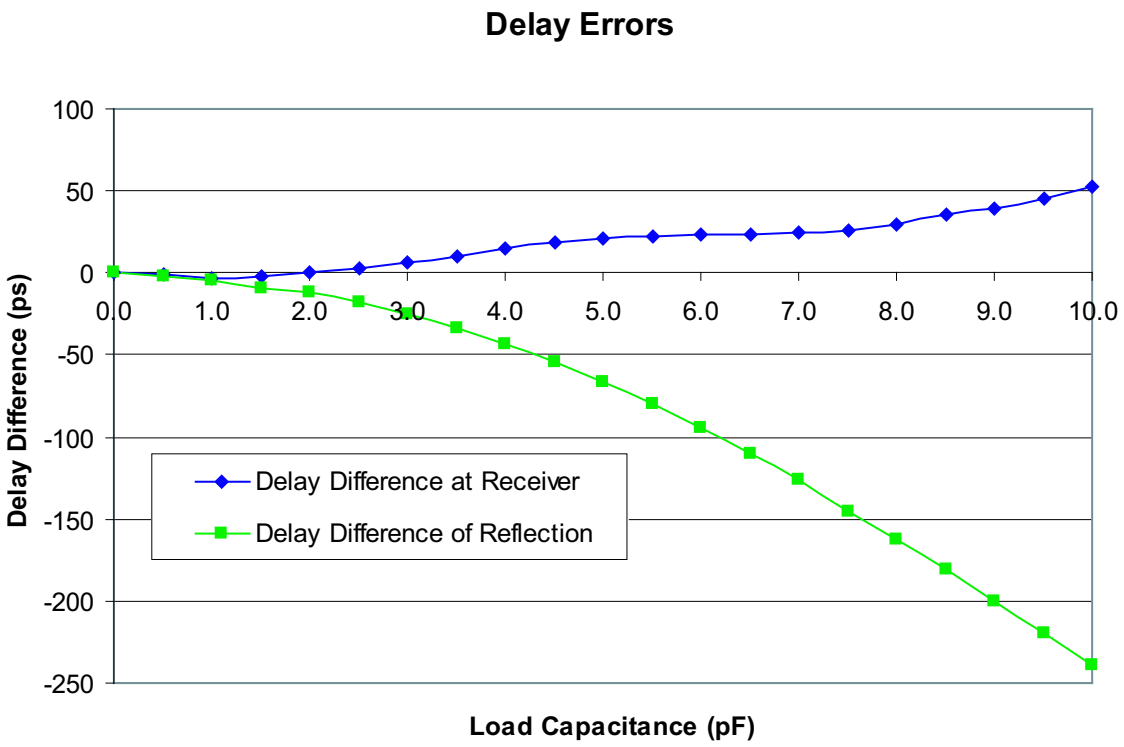

Figure 55: Reflection delays for several loads and equivalent lengths.

The error introduced by the capacitive termination is shown in Figure 55. At very high loads the delay error introduced by the load can exceed 200 ps. This is due to the fact that lines with very heavy capacitive loading exhibit substantial reduction in the rise time of the reflected signal. From this result, it can be seen that differences in load capacitances can dominate system resolution in some cases. If the error introduced by the load exceeds the system resolution, the error will limit the system characteristics after correction. However, the deskewing system can still substantially reduce the overall skew. For the system presented here, the effects of loading become a limiting factor in system resolution when the total difference in load capacitances is approximately 6 pF.

3.5.3 System Interaction

A simple model has been developed for predicting the effects of capacitive loading on the deskewing system. A large capacitive load is seen as an extension of the line length at the transmitting end of the line and will be deskewed as if the line has an additional length given by Equation 66. The difference in delay that is measured from the reflections will deviate from the difference in delay seen at the receiver for heavily loaded lines, as illustrated in Figure 55. The effect this has on the open-loop deskewing system will now be examined through simulation.

For the simulation, eight lines are identical length are each terminated with a different load capacitor. Each load will produce a different skew at the receiver. To measure skew, the first line is left with 0 pF load and the delay between the midpoint voltage of the first trace and the remaining traces is measured. In addition, the lines are then deskewed using the open-loop deskewing system described. The skew at the loads before and after deskewing as well as the theoretical skew predicted by the model are shown in Figure 56. The loads here have been chosen to be 0 pF, 1 pF, 2 pF, 3 pF, 4 pF, 5 pF, 6 pF, and 7 pF, where the magnitude of the load increases by 1 pF for each line in increasing order. As evident in the figure, the predicted and simulated skews match very closely for most loads. Significant deviation occurs primarily for large loads ($> 6\ pF$), and is due primarily to neglecting the series inductance when computing an equivalent length. Before deskewing, the differences in load values create a skew at the receiver of approximately 300 ps at the midpoint voltage. The open-loop system reduces this skew to approximately 100 ps.

System level simulation of the open loop system in the presence of disparate loading on the lines has verified the model described earlier. As expected, the loading makes the lines appear to have a length that is greater than their actual physical length. The deskewing system compensates for this apparent difference and reduces the skew appropriately. However, the loading creates differences between the delay at

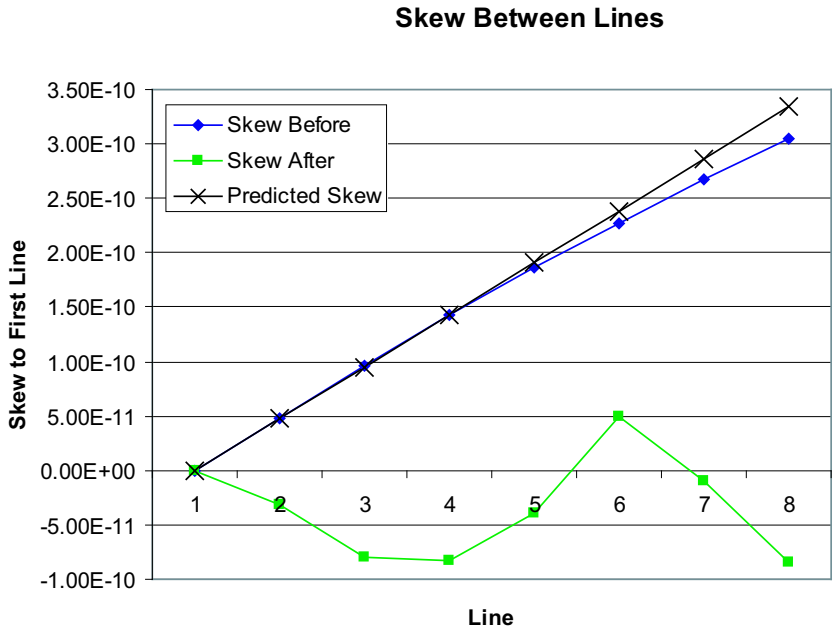

Figure 56: Simulated and predicted skew between traces at the receiver end of the traces and skews after deskewing.

the receiver and for the reflections, resulting in a somewhat worse than ideal corrected skew. This error is expected, based on the results shown in Figure 55, but is still not too large a deviation from the ideal results.

CHAPTER IV

LIMITATIONS OF AN OPEN-LOOP DESKEWING SYSTEM

The functionality of an open-loop deskewing system has been demonstrated experimentally, indicating the resolution of this system to be approximately 90 ps. This result, however, applies only to the particular system that was fabricated. The resolution of the architecture, in general, will scale with process technology and will be limited by several factors, as described below. In general, these factors will be one of three basic types: those relating to delay measurement, those relating to delay correction, and those relating to non-idealities in the PCB traces.

4.1 Delay Measurement

The primary and most fundamental limitation of the open-loop deskewing system is the measurement process. For delay measurement, a set of counters are used to count the number of edges produced by an oscillator in the appropriate period. The number of edges indicates round trip delay through each trace. The oscillator design will determine the minimum time step that can be measured and also sets the performance requirements of the counters. The limitations of this system will be considered in two components: the oscillator, which sets the minimum time step, and the counters, which can become a limiting factor when used with high frequency oscillators.

4.1.1 Measurement Time Step

Ring structures have become a popular choice for oscillator design in modern systems. This is due to the fact that a ring oscillator can be easily implemented in a standard CMOS process and will require less area than an LC oscillator. In addition, a ring oscillator provides a wide tuning range and several output phases. For use in this open-loop deskewing system, it is the availability of multiple output phases that provides a distinct advantage.

4.1.1.1 Ring Based Design

In a multiple phased system, the number of edges produced by every phase can be counted. In the time domain, the delay between a transition at the input of any stage and a transition at the output of the same stage will be equal to the delay through that single stage. This is the minimum time step that can be measured. For example, a three-stage ring oscillator provides a minimum measurable time step that is equal to one sixth the oscillator period, since this corresponds to the delay through a single stage of the ring. In general, the minimum resolution available from an N-stage ring oscillator will be equal to

$$t_{min,ring} = \frac{T_{ring}}{2 \times N} \tag{70}$$

where T_{ring} is the period of the oscillator. The factor of 2 arises from the fact that each period includes both a rising and a falling edge. The factor of N arises from the ability to take advantage of the N available phases of the oscillator. Using a faster oscillator with the same number of stages will directly provide a proportional increase in the measurement resolution, corresponding to a reduction in T_{ring} in Equation 70. For example, switching from a 3-stage 2.2 Ghz ring oscillator (T_{ring} = 450 ps) to a 3-stage 4.4 GHz ring oscillator (T_{ring} = 225 ps) in the same process will allow the system to measure a minimum time step of 37.5 ps (= 225/6 ps), which is half the current minimum resolution of 75 ps (= 450/6 ps).

4.1.1.2 LC Based Design

The second major type of oscillator used in modern systems is an LC oscillator. These oscillators are built using passive resonant elements, and may have very high Q factors. This results in generally better phase noise and increased frequency performance as compared to ring oscillators. For application in this open-loop deskewing system, however, the increased frequency is not necessarily an advantage. Whereas ring oscillators provide several output phases, an LC oscillator will provide only a single output phase. Therefore, the minimum resolution available from an LC oscillator will be

$$t_{min,LC} = \frac{T_{LC}}{2} \tag{71}$$

where T_{LC} is the period of oscillation. Comparison of Equations 70 and 71 provides the condition necessary for both oscillators to provide the same measurement resolution,as shown

$$t_{min,ring} = t_{min,LC} \tag{72}$$

$$\frac{T_{ring}}{2 \times N} = \frac{T_{LC}}{2} \tag{73}$$

giving

$$T_{ring} = N \times T_{LC} \tag{74}$$

This result indicates the LC oscillator must be at least N times faster than the ring oscillator to provide the same measurement resolution.

Assuming that both oscillators could be built to provide an identical measurement resolution, the ideal choice is still unclear. Because the ring oscillator requires counting of N phases, the ring oscillator based system will require N times as many counters. However, having a slower operating frequency relaxes the performance requirements on the counters and allows the same measurement range with fewer counter bits (see Equation 14). The LC oscillator, on the other hand, will require

only two counters, one for the rising edges and one for the falling edges. These counters, however, must operate N times as fast as the counters for the ring-based design (see discussion below) and must have a slightly larger number of bits.

4.1.1.3 Generalized Results

Ring-based oscillators and LC oscillators are fundamentally different. The choice of a particular oscillator type has several important consequences for the system level design and performance limitations, such as measurement resolution, the number of counters required, the performance requirements and bit width of the counters. Therefore, a generalized result that can be used to incorporate the design criteria and performance implications of both types of oscillators is desirable to aid in a system level comparison of the impact of a particular oscillator choice. As a generalization, the LC oscillator can be considered to be a single stage ring oscillator. Using this assumption, the design criteria can be summarized, as shown in Table 5, where t_d is the maximum one-way delay through a PCB trace and N is the number of stages of a ring oscillator or 1 for an LC oscillator.

Table 5: Delay Measurement Summary

Criteria	Value
Measurement Resolution	$\frac{T_{oscillator}}{2\times N}$
Counters Required	2×N
Counter Switching Frequency	$\frac{1}{T_{oscillator}}$
Counter Bit Width	$\lfloor log_2\left(\frac{2t_d}{T_{oscillator}}\right)\rfloor$

4.1.2 Digital Logic

Assuming that an arbitrarily fast oscillator can be built, the next bottleneck in system resolution occurs at the delay measurement circuitry. Since the number of pulses generated must be counted in order to get a digital representation of the line length, a digital counter must necessarily be included in the system. This counter must be able to change state at the same frequency as the oscillator, as a minimum requirement.

In practice, the counter should be able to run even faster to account for possible peak-to-peak jitter in the oscillator output. For example, a 10 GHz oscillator will require a counter that can run at 10 GHz. For a ring-oscillator based system, this frequency requirement will not typically restrict system resolution. The period of the ring oscillator will be at least two gate delays, which is an adequate minimum input pulse for a standard counter. The LC oscillator based design, however, presents a larger challenge. Since this oscillator must run N times faster than the ring-oscillator design, the counters for the LC oscillator based design must also be N times as fast. For example, in a 0.25 μm process, a 2.2 GHz ring oscillator requires counters that can run at 2.2 GHz. This is easily accomplished using static CMOS techniques. An LC oscillator in the same process needs to run at 6.6 GHz to achieve the same resolution, therefore requiring counters that run at 6.6 GHz. In a 0.25 μm process, static CMOS techniques cannot be scaled to this frequency. Instead, a more aggressive technique, such as a low voltage differential current mode logic (CML) technique, would be necessary. Even this, however, may not be adequate to meet the performance requirements of the LC oscillator. In general, the availability of an adequately fast counter will depend on the particular application (process, design technique, and oscillator frequency). If an adequate counter cannot be built, then a ring oscillator based design must be used.

4.2 Delay Correction

The second part of the system that imposes limits on resolution is the delay correction circuitry. The VCDL in this system is designed with a delay quantization factor that corresponds to the measurement quantization factor. Each delay block in the VCDL is scaled to provide a very specific delay that is determined during design. Since the system runs in open loop, any variation in the VCDL delays will not be known to the system and cannot be compensated for automatically. These variations in the actual

cell delays away from the expected values will appear directly as skew at the output.

4.2.1 Process Variations

One of the fundamental limitations of this open-loop system is its susceptibility to shifts in process parameters. Random process variations between devices and broad shifts in device parameters will cause the actual delay provided by any particular delay cell to vary slightly. This difference in delay limits the minimum resolution achievable by the entire system.

Simulation results of the delay for each block of the VCDL are shown in Figure 57. The delays have been normalized against the delay expected for a typical-typical process. Simulations were run for fast-fast (ff), fast-slow (fs), slow-fast (sf), and slow-slow (ss) process corners. All simulations were run at the same power supply and temperature to explicitly demonstrate the effect of broad process shifts on the delay line. As evident in the figure, process shifts can cause variations of up to 20% away from the expected values. The exact variation will depend on the process parameters of the particular fabrication run as well as the circuit techniques used to create the delays. In general, variation of the delay through a particular block away from the expected value will contribute skew to the signals after programming.

4.2.2 Temperature Variations

Temperature variations impact overall system resolution in the same manner as process variations. Shifts in system temperature cause the actual delay through any particular cell to deviate from the expected delay. In general, inverter chains switch faster at lower temperatures and slower at higher temperatures. Since this system does not have built-in temperature compensation, the error introduced by changes in switching speeds will appear directly as skew at the receiving chip. Simulation results of the delay for each cell in the delay line for cold (0 °C) and hot (150 °C) temperatures are shown in Figure 58. The delays have been normalized against a

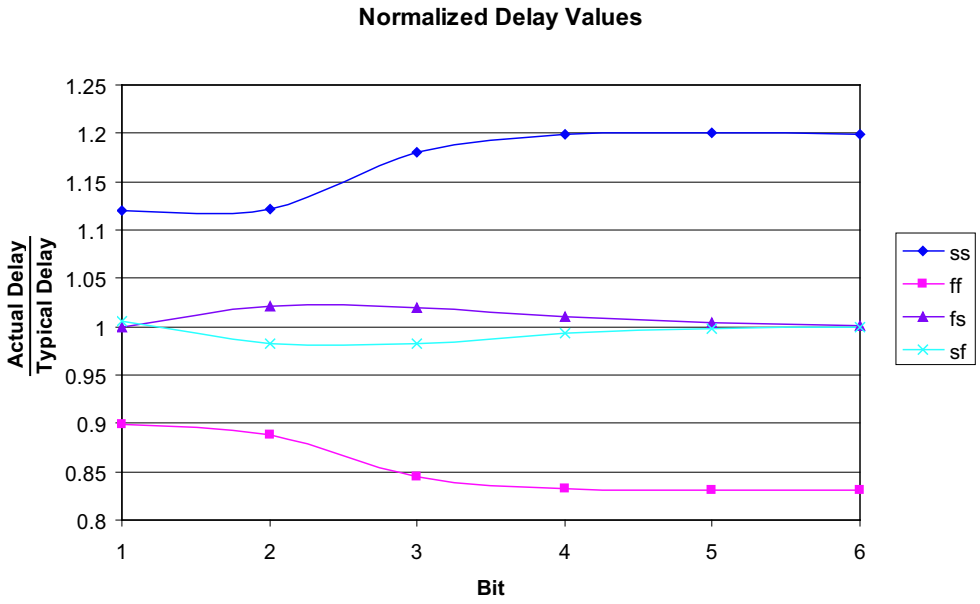

Figure 57: Normalized delay line values across process corners.

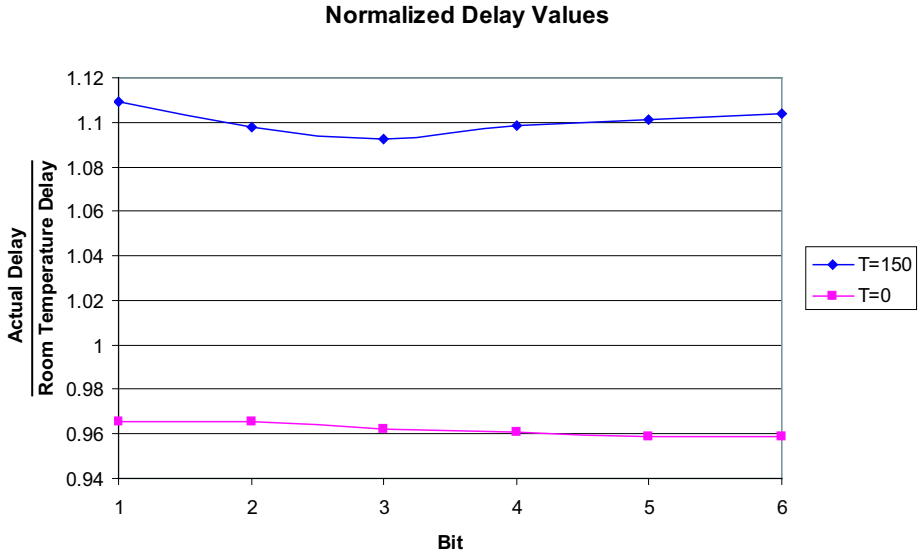

Figure 58: Normalized delay line values for several temperatures.

room temperature (27 °C) simulation. Simulation results indicate that temperature variation will cause the delay through a particular cell to vary up to 15% from the expected value.

4.2.3 Power Supply Variations

The third major contributor of delay variations is power supply fluctuations. In a standard application, the power supply supplied to a particular chip may vary as much as ±10%. For example, the TSMC 0.25 μm process used to fabricate the test chip for the open-loop deskewing system is intended to run at 2.5 V power supply. However, in actual use the chip may receive anywhere from 2.25 V to 2.75 V. The delay through the delay line is strongly dependant on the power supply voltage. Running at a higher than expected power supply voltage results in delays that are less than the design values. Once again, this deviation in delay values away from the design values appears directly as skew at the receiving chip.

Simulation results of the delays for each of the six delay blocks are shown in Figure 59 for high (2.75 V) and low (2.25 V) V_{dd} values. As expected, the high V_{dd} results in delays that are less than expected while the low V_{dd} results in delays that are higher than expected. The magnitude of the impact of V_{dd} variation depends on the specific implementation of the delay differences in each cell and will not impact every design in an identical manner.

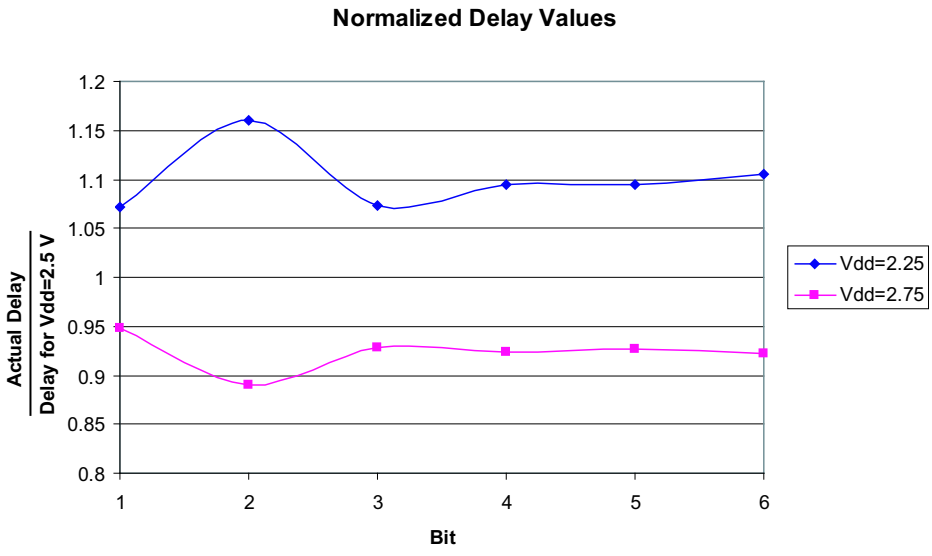

Figure 59: Normalized delay line values for several Vdd values.

4.3 Line Effects

The third major source of limitations for this system is PCB trace effects.

4.3.1 Dispersion

The first error source introduced by the PCB traces is dispersion. The effect of dispersion in this application is to cause the reflected voltage waveforms to have a much larger rise time than the transmitted signals. If the detector for every line and the dispersion experienced by every pulse are identical, then this will not be a problem. In practice, however, this is not the case. Random process variations between devices cause mismatch in the threshold voltages (V_T) between devices. In a level-sensitive detector, shifts in V_T will cause shifts in the trip point. The shift in the voltage trip point causes a shift in the time domain, changing the apparent delay through the line. This effect is illustrated graphically in Figure 60. As a simple approximation, consider the slope during the rise of the reflected pulse to be constant, corresponding to the diagonal line in Figure 60. The slope of this line will be give by

$$slope = \frac{V_{dd}/2}{t_r} \tag{75}$$

where t_r is the rise time of the reflected pulse. The shift in the measured delay will then be equal to

$$\Delta T = \frac{\Delta V_T}{slope} = \frac{\Delta V_T \; t_r}{V_{dd}/2} \tag{76}$$

This result indicates that the time shift introduced by dispersion will be directly proportional to the rise time of the reflected pulse. Longer lines exhibit greater dispersion and will therefore introduce a proportionately greater error into the measurement process.

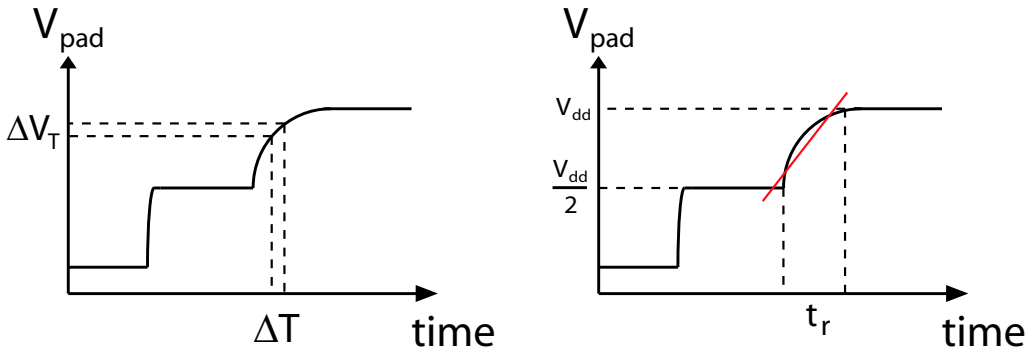

Figure 60: Illustration of the impact of dispersion on the open-loop deskewing system.

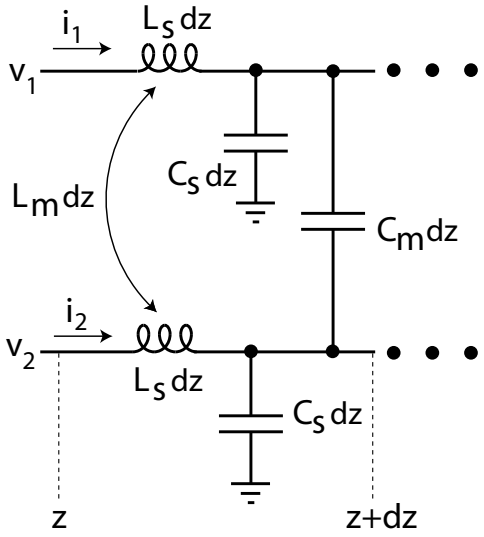

Figure 61: Circuit model of a differential line element including mutual inductance and capacitance.

4.3.2 Inductive and Capacitive Coupling

4.3.2.1 Theory

Another major error source introduced by the PCB traces is inductive coupling between the traces. In general, a pair of PCB traces can be modelled using the circuit in Figure 61 [30]. For this discussion, it is assumed that the series resistance is very small, as is typically the case for a PCB trace, and has therefore not been included in the model for simplicity. This circuit represents a differential length of a pair of PCB traces with a total inductance of L_s, a total capacitance of C_s, a mutual inductance

between the lines of L_m, and a mutual capacitance between the lines of C_m. From this circuit, the voltage and current can be described as

$$\frac{d}{dz}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_s & L_m \\ L_m & L_s \end{bmatrix} \frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{77}$$

$$\frac{d}{dz}\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} C_s + C_m & -C_m \\ -C_m & C_s + C_m \end{bmatrix} \frac{d}{dt}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{78}$$

What these equations say is that a the voltage on one line depends not only on the inductance and capacitance per unit length of that line, but also on the coupling between that line and any adjacent lines. The noise caused by the mutual inductance and capacitance is commonly referred to as crosstalk.

An empirical estimation of the mutual inductance between two lines is given by [30]

$$\begin{aligned} \frac{L_m}{\mu_0} = &\left[-4.15\left(\frac{H}{W}\right)^{-0.16} - 2.38\left(\frac{T}{W}\right)^{1.18} \right] \cdot \left(\frac{S}{H} + 1.07\right)^{-2.6} + \\ &\left(\frac{S}{H} + 0.89\right)^{-2.03} \cdot \left[0.418\left(\frac{H}{W}\right)^{0.13} + 1.37\left(\frac{T}{W}\right)^{1.09} \right] \end{aligned} \tag{79}$$

where S is the spacing between the traces, H is the dielectric thickness, W is the width of the traces, and T is the trace thickness. The mutual capacitance will be given by

$$\begin{aligned} \frac{C_m}{\epsilon_0} = &1.17\left(\frac{W}{H}\right)^{0.083} \cdot \left(\frac{S}{H} + 0.402\right)^{-0.78} + \\ &\left(\frac{S}{H} + 1.32\right)^{-0.8} \cdot \left[-1.36\left(\frac{W}{H}\right)^{-0.037} + 0.227\left(\frac{T}{H}\right)^{0.98} \right] \end{aligned} \tag{80}$$

These equations are shown in literature to match both purely analytical and experimental results. If exact PCB trace dimensions are known, exact analytical equations could be used. This discussion, however, attempts to address the general problem and will not focus on one particular set of dimensions, so the simple, empirical equations will suffice.

For simulation, the entire line is modelled using N differential line segments, where each is described by the lumped element circuit in Figure 61. Using a larger N results in the values of the discrete elements becoming smaller and the total netlist consisting of a greater number of line segments. As a result, the line begins to exhibit a more distributed behavior that becomes a better approximation of a physical PCB trace characteristic. Therefore, N will typically be chosen to be a large number and may be up to 100 for a good simulation.

For the deskewing system, crosstalk can introduce errors into the reflected waveforms. For the open-loop deskewing system, all the lines are initially pulsed simultaneously. In this case, the forward propagating waveforms will be identical and the mutual inductance and capacitance will have no effect. The errors introduced by mutual inductance and capacitance will appear in the reflected waveforms between lines with different lengths. From Equation 79, using the the PCB dimensions from Table 2 and a minimum spacing of $S = 7$ mils gives

$$L_m = 1.04\,\text{nH/inch} \tag{81}$$

The mutual capacitance for the same line is found to be

$$C_m = 0.035\,\text{pF/inch} \tag{82}$$

When compared to the inductance and capacitance per unit length, which have typical values of

$$L_s = 7.5\,\text{nH/inch} \tag{83}$$

$$C_s = 3\,\text{pF/inch} \tag{84}$$

it can be seen that

$$\frac{L_m}{L_s} = 0.138 \tag{85}$$

$$\frac{C_m}{C_s} = 0.017 \tag{86}$$

Table 6: PCB Trace Characteristics

Characteristic	Value
Impedance	50 Ω
L_s	7.5 nH/inch
C_s	3 nH/inch
Line 1 Length	3 inches
Line 2 Length	4 inches
Load Capacitance	2 pF
Package Inductance	5 nH
Package Capacitance	2 pF

This implies that the effect of the mutual inductance will be dramatically greater than the effect of the mutual capacitance. Therefore, this discussion will focus on the effects of mutual inductance between lines. For this discussion, the coupling coefficient, cc, represents the coupling between the inductances per unit length of the PCB traces and will be given by

$$cc = \frac{L_m}{L_s} \tag{87}$$

4.3.2.2 Characterization

Mutual inductance between lines introduces error into the deskewing system by making the skew between the reflections a function of more than just the propagation delays through the lines. Factors such as line spacing and the coupling coefficient become critical when considering signal reflections. For example, consider the simulation results shown in Figure 62. For this simulation, two adjacent microstrip lines with the characteristics shown in Table 6 are simultaneously pulsed using an ideal 50 Ω driver with a rise time of 500 ps. Several simulations were run using different coupling coefficients, ranging from $cc = 0$ to represent no coupling to $cc = 0.8$, which is several times a worst case coupling estimation and is purely for illustration. For this experiment, the lines are simulated using $N = 100$ differential line segments to closely approximate the behavior of a real microstrip trace. As evident in Figure 62, the mutual inductance between the lines causes shifts in the reflected

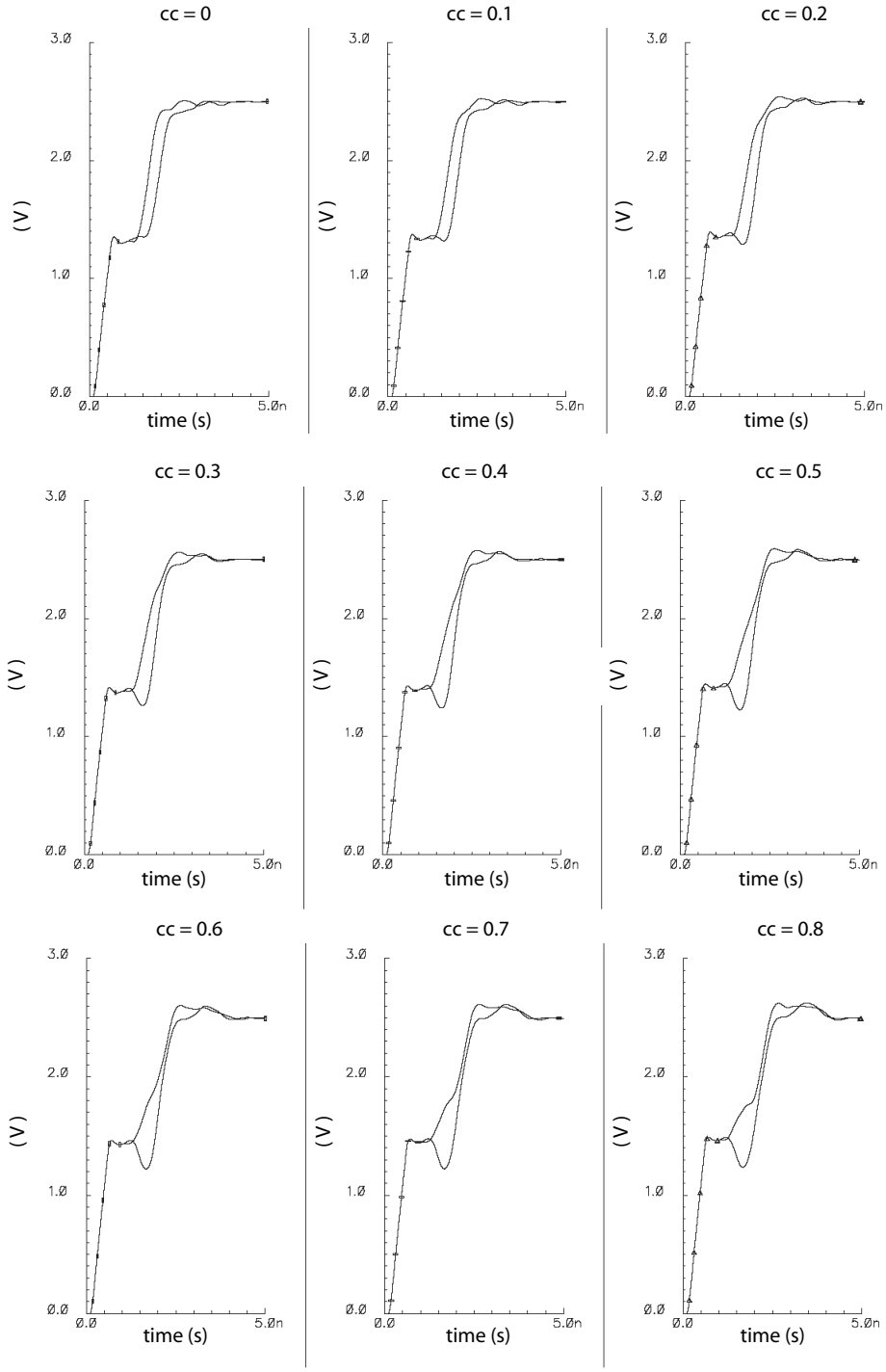

Figure 62: Transient simulation results for two lines with varying mutual inductance values.

waveforms, thereby obscuring the information about the trace propagation delays that the reflected waveforms should carry. The actual skew between the lines should

be approximately 300 ps. The measured skew will be some amount less than this, depending on the magnitude of the coupling coefficient. If a typical value of *cc* is between 0.1 and 0.2 for microstrip traces with normal dimensions, then the effect of mutual inductance is minor - a variation of only a few picoseconds in the overall measurement. Large variations tend to occur for *cc* values greater than about 0.3. A coupling coefficient value of 0.3 represents very strong coupling between the lines.

The question then becomes how inductive coupling impacts the performance of the deskewing system. The exact impact of coupling will depend on the particular configuration of the PCB traces - including the trace dimensions, length, and spacing. In particular, the issue that must be addressed is the impact of inductive coupling on the measured round-trip delay as compared to the actual one-way delay. Since the system deskews one-way delays based on measured round-trip delays, errors in the measured delay will result in skew at the receiver.

For a test case, consider an eight-line system where every line is of a different length and all the lines are adjacent. For a worst case estimate, the line lengths are chosen to be 1, 2, 3, 4, 5, 6, 7, and 8 inches. Each line is coupled inductively to each adjacent line (for example, line 1 is coupled only to line 2 and line 2 is coupled to lines 1 and 3). Coupling between nonadjacent lines is negligible by comparison. Ideally, the measured round-trip delay should be equal to exactly twice the one-way delay through the trace. Inductive coupling between the lines, however, will alter this ratio. The ratio of the round-trip delay (measured at 2.0 V) to the one-way delay (measured at $V_{dd}/2 = 1.25\,V$) is shown in Figure 63 for several values of the coupling coefficient.

As evident in the figure, inductive coupling distorts the delay ratio. As the coupling coefficient increases, the magnitude of the error also increases. In particular, the greatest percentage error is for the shortest lines, where a small time difference can be a relatively large fraction of the total delay. The error measured as a time

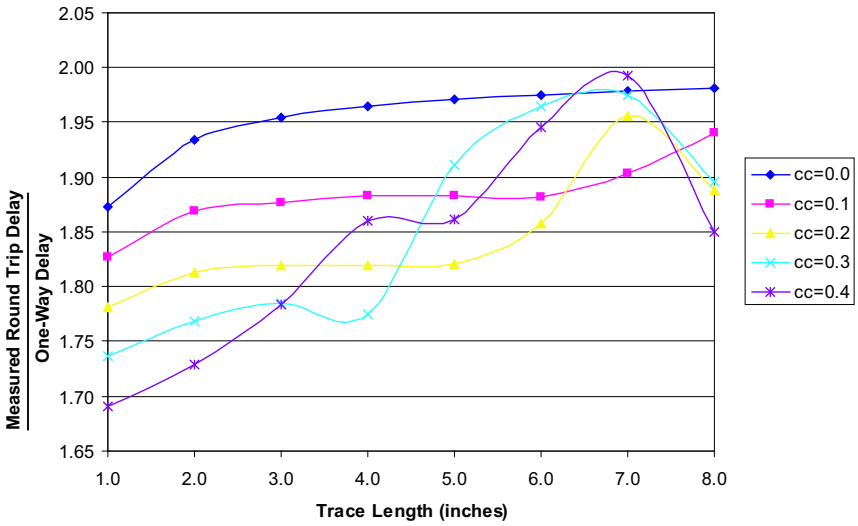

Figure 63: Ratio of the measured round trip delay to the one-way delay for several values of the inductive coupling coefficient for an eight-line system.

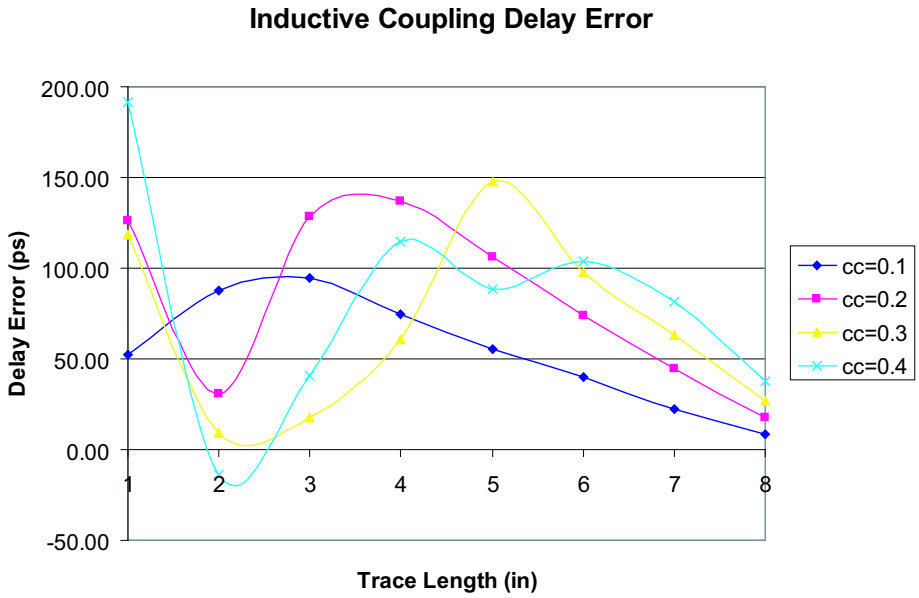

Figure 64: Delay error caused by inductive coupling.

period is shown in Figure 64. The error is defined as

$$error = T_{round-trip} - 2 \times T_{one-way} \tag{88}$$

where the error for $cc = 0$ has been normalized to 0 ps. The error introduced by

inductive coupling is less than 200 ps for values of cc less than 0.4, which is several times the coupling expected for typical PCB dimensions. For typical PCB dimensions and spacings (i.e. $cc \approx 0.1$), the error is less than 100 ps.

4.3.2.3 System Interaction

To investigate the impact of inductive coupling between lines on the open-loop deskewing system, characterization is performed in simulation. For the simulation setup, an eight-bit open-loop deskewing system is setup with eight lines of different length. The lines are chosen to be 1, 2, 3, 4, 5, 6, 7, and 8 inches. Each line is coupled only to the adjacent lines. To isolate the effects of inductive coupling, simulation is performed without any package parasitics. The lines are modelled using the circuit in Figure 61. The signal waveforms at the receiver after deskewing are shown in Figure 65. The system behaves as expected for when there is no coupling between the lines ($cc = 0.0$) - all the waveforms are closely aligned and the edge rates are very steep. As the coupling coefficient increases, more error is injected into the final solution, increasing the skew at the receiver after programming.

4.4 Power Supply

The open-loop deskewing system described here is implemented using only standard static CMOS techniques and a single three-stage ring oscillator. All of the circuits used can be implemented in a low-voltage technology with minimal modifications to the reflection detectors and the oscillator. The circuitry is, in general, not restricted by the power supply voltage.

The limitation arising from decreasing V_{dd} arises in detecting the reflected waveforms. As discussed in Section 3.3.7, the noise margin of the detectors is a fraction of the power supply. Therefore, decreasing the supply voltage will reduce the noise margins of the system. For example, a 1 V system will have a noise margin of only

250 mV. The overshoot caused by parasitic inductance could easily be 100 mV, leaving only a 150 mV margin for all other error sources, such as V_{dd} fluctuations or driver and trace impedance mismatch.

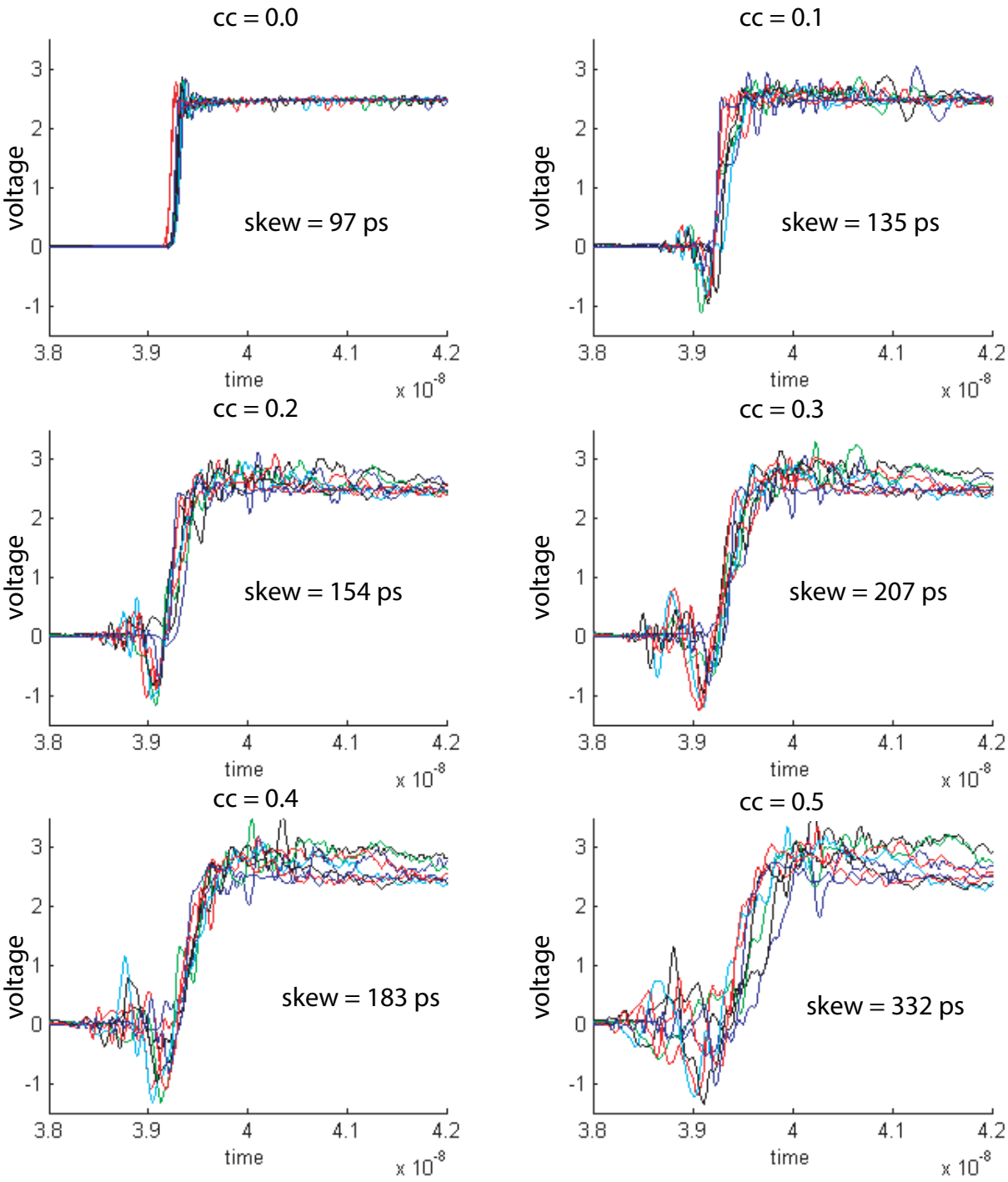

Figure 65: Simulated waveforms at the receiver after deskewing for several degrees of inductive coupling between lines.

CHAPTER V

A SYSTEM FOR DESKEWING A DIFFERENTIAL PAIR OF LINES

Many modern high-speed digital systems use differential techniques for high speed signal transmission. Differential signals have several advantages over single-ended signals, such as increased edge rates and greater immunity to noise. To transmit differential signals, two conductors are needed - one for the positive signal and one for the negative signal. If the delay through each of the lines is different, then the differential signal at the receiver will be distorted, resulting in a slower data transmission rate for the entire system or potentially causing data transmission errors. The delay between two lines can easily become different in a standard PCB design. Random mismatch between the lines can cause the capacitance or inductance per unit length to be different. In addition, delay differences arise from differences in trace length and loading. If two traces run adjacent to each other, then a turn in the path will cause the total lengths of the lines to be different. Even small differences in the trace delays can cause substantial problems for systems with small timing margins.

This chapter presents an architecture to deskew signals transmitted through a pair of differential microstrip lines. In general, when a pair of 50 Ω PCB traces is used to transmit a differential signal to another chip, the traces will be terminated by a 100 Ω resistor at the receiver, as shown in Figure 66. For a perfect differential signal, the 100 Ω resistor behaves as if it has a virtual ground at its center and provides a 50 Ω matched termination for each line. If the differential signal is distorted due to delay mismatch between the traces, however, the virtual ground will not exist,

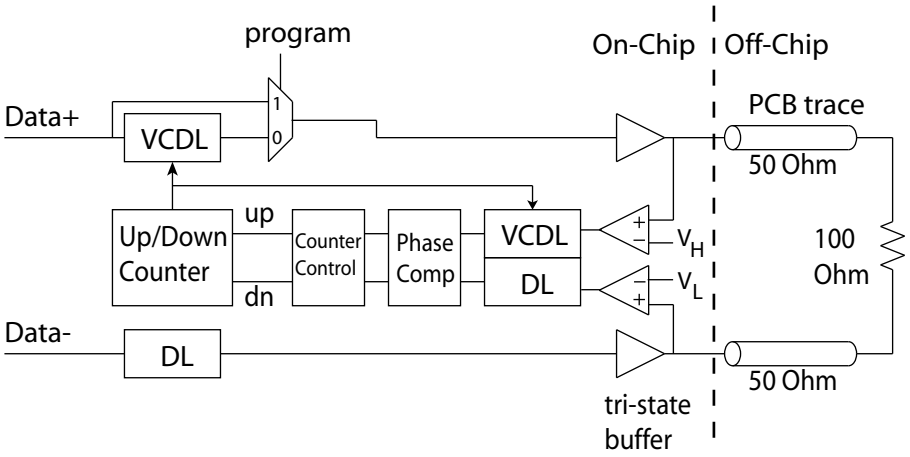

Figure 66: Proposed architecture of the differential deskewing system.

resulting in unmatched terminations and signal reflections on the lines. The existence of a termination to the lines presents an additional challenge to the use of TDR techniques. Specifically, the magnitudes of any reflected signals will be less than that of the transmitted signals, reducing the system noise margins. In addition, pulses from both ends of the differential lines will propagate past the terminating resistor if the lines are not perfectly terminated or if the traces are of different lengths.

To correct for the difference in delay for a pair of differential lines, an iterative technique is used to add or remove delay to the positive signal path until the skew between the lines has been eliminated. Time domain reflectometry is used to compare the delays through the lines.

5.1 System Description

5.1.1 System Architecture

Figure 66 shows a block diagram of the proposed differential deskewing system. A counter controlled digital delay-locked-loop (DLL) is set up around a voltage controlled delay line (VCDL) and the positive PCB trace of the pair. A fixed delay line (DL) in series with the negative PCB trace is used as a fixed delay. On each pulse, the delay through the VCDL and positive PCB trace is adjusted until the delay exactly

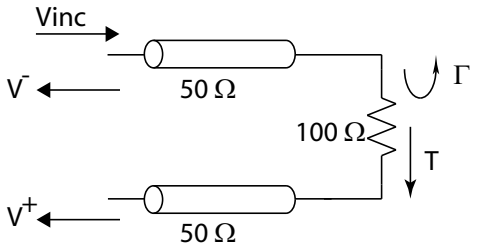

Figure 67: Circuit model for a terminated pair of differential lines

matches the delay through the fixed delay line and the negative PCB trace and a lock is achieved. For this system, one can calculate the delay from the data inputs, through the delay lines and output buffers, to the receiving chip for the positive (T^+) and negative (T^-) lines. These total delays will be given by:

$$T^+ = T_{vcdl} + T_{buf} + T_{ustrip,p} \tag{89}$$

$$T^- = T_{dl} + T_{buf} + T_{ustrip,n} \tag{90}$$

Where T_{vcdl} is the delay through the VCDL, T_{buf} is the delay of the output drivers, $T_{ustrip,p}$ is the delay through the positive microstrip line, and $T_{ustrip,n}$ is the delay through the negative microstrip line. It has been assumed here that both output drivers are identical and have exactly the same delay. In practice, random mismatch between the drivers will cause the delay through the drivers to be slightly different.

To compare the delays through the PCB traces, the negative output driver is placed into a high-impedance mode and the positive output is pulsed repeatedly using the Data+ input. Each pulse travels down the positive line and reaches the terminating resistor. At the resistor, the pulse is partially reflected back down the positive line and partially transmitted down the negative line, as shown in Figure 67. The reflection and transmission coefficients at the end of the line are given by Equation 91 and 92.

$$\Gamma = \frac{(R_L + Z_o) - Z_o}{(R_L + Z_o) + Z_o} = \frac{1}{2} \tag{91}$$

$$T = 1 + \Gamma = \frac{3}{2} \tag{92}$$

Where Z_o is the trace impedance (ideally 50 Ω) and R_L is the resistance of the terminating resistor (ideally 100 Ω). The magnitudes of the reflected and transmitted pulses are then calculated as shown in Equation 93 and 94.

$$V^- = \Gamma \times V_{inc} = \frac{1}{2} V_{inc} \tag{93}$$

$$V^+ = T \times V_{inc} \times \frac{Z_o}{R_L + Z_o} = \frac{1}{2} V_{inc} \tag{94}$$

where V_{inc} is the magnitude of the incident pulse. These reflected and transmitted pulses travel back to the chip and are detected on-chip using an appropriately tuned detector on each line. The detectors in this implementation are realized using comparators with one input tied to a DC level [1, 19]. By adjusting the DC level, the detect voltage can easily be adjusted to the correct value. Comparators are used instead of Schmitt triggers in this implementation because comparators exhibit an easily tunable trip point while not sacrificing a fast switching characteristic. A comparator, however, draws a DC current and consumes more power than a Schmitt trigger circuit. The relative phase between the outputs of the two detectors indicates the difference in delays through the two PCB traces. For the system to achieve a lock, however, the delay through each trace plus the delay through the corresponding delay line must be compared. Therefore, the output of each detector is passed through a replica of the corresponding delay line before the relative phase between the signals is compared [21, 40]. The total times required for the signals to travel from the terminating resistor to the phase comparator for the positive ($T_{reflect+}$) and negative ($T_{reflect-}$) lines are given by:

$$T_{reflect+} = T_{ustrip,p} + T_{detect} + T_{vcdl} \tag{95}$$

$$T_{reflect-} = T_{ustrip,n} + T_{detect} + T_{dl} \tag{96}$$

Where T_{detect} is the delay through a detector and it has been assumed that the delays through the detectors for both lines are identical. When the system achieves a lock,

$T_{reflect+}$ and $T_{reflect-}$ will be identical. At this point,

$$T_{ustrip,p} + T_{detect} + T_{vcdl} = T_{ustrip,n} + T_{detect} + T_{dl} \tag{97}$$

which leads to

$$T_{ustrip,p} + T_{vcdl} = T_{ustrip,n} + T_{dl} \tag{98}$$

Substituting this result back into Equations 89 and 90 gives the following.

$$T^{+} = T_{vcdl} + T_{ustrip,p} + T_{buf} = T_{ustrip,n} + T_{dl} + T_{buf} = T^{-} \tag{99}$$

When this occurs, $T^{+} = T^{-}$ and the data will be synchronized at the receiver.

5.2 Implementation

The deskew system in Figure 66 consists of a VCDL, fixed delay line (DL), phase comparator (PC), up/down counter, a counter control block to interface the PC to the counter, output drivers, and reflection detectors. The up/down counter is built using standard static CMOS techniques. The output buffer is simply an inverter scaled to have an equivalent 50 Ω impedance while driving the PCB trace. The remaining circuits will be described as follows.

5.2.1 Phase Comparator

Many conventional phase comparators are limited by a dead zone, where the PC cannot determine the relative phases of its inputs. To overcome this, a precharge-type phase comparator is used [21, 40], as shown in Figure 68. If the X signal leads the Y signal, then the output will be low until Y rises. Otherwise, the output will remain continuously high. The timing diagram of these events are shown in Figure 69.

Since the structure in Figure 68 can only detect if X leads Y, two of these structures are used to create the complete phase comparator [21,40], as shown in Figure 70. In this way, the relative phase of the inputs can always be determined.

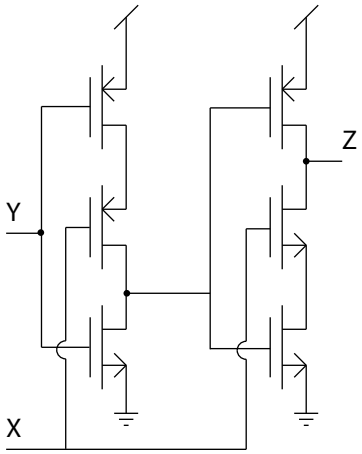

Figure 68: Precharge-type phase comparator.

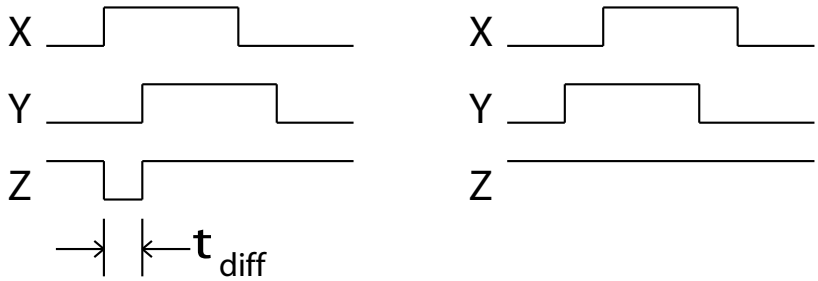

Figure 69: Phase comparator timing diagram.

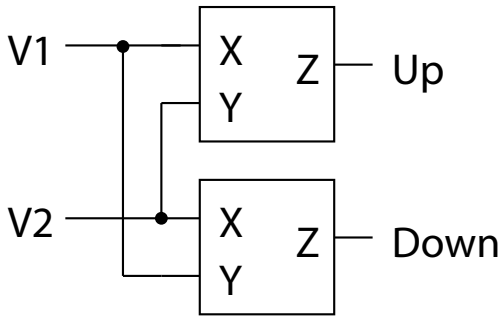

Figure 70: Phase comparator block diagram.

5.2.2 Counter Control

The purpose of the counter control block is to allow the PC to interface to the up/down counter. The width of the output of the PC depends on the skew between the PC inputs and becomes arbitrarily small as the inputs become deskewed. The counter clock input, however, requires a minimum pulse width for proper operation.

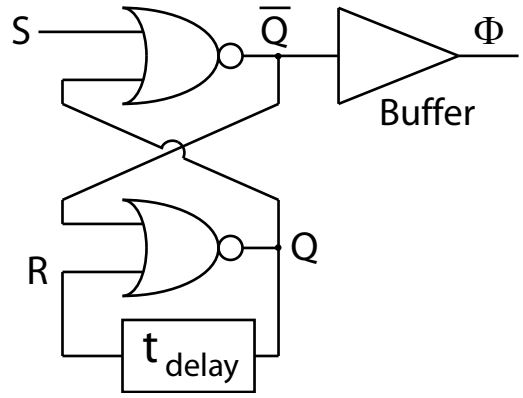

Figure 71: Counter control circuitry.

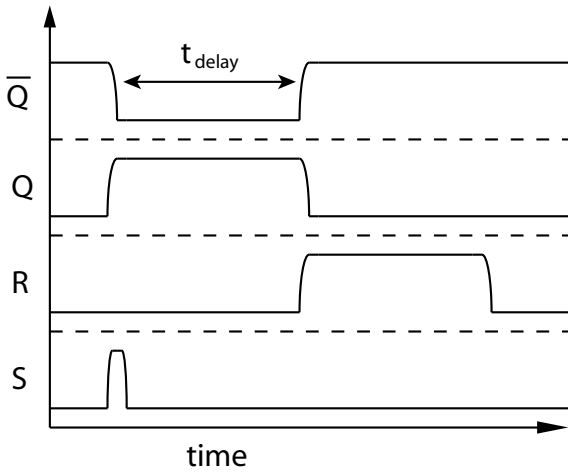

Figure 72: Counter control waveforms.

To ensure a minimum pulse width for the counter input the circuit in Figure 71 is used. A timing diagram of this circuit's output is shown in Figure 72. In this circuit, an input pulse on the S line of arbitrarily small width triggers an output pulse of width equal to t_{delay}.

5.2.3 Delay Line

Figure 73 shows the structure of the binary weighted VCDL [7]. The VCDL consists of a number of a cascade blocks, with each block being tuned to a binary weighted delay as indicated by the multipliers. The number of blocks corresponds to the number of control bits of the VCDL. The maximum delay block is set by the number of bits

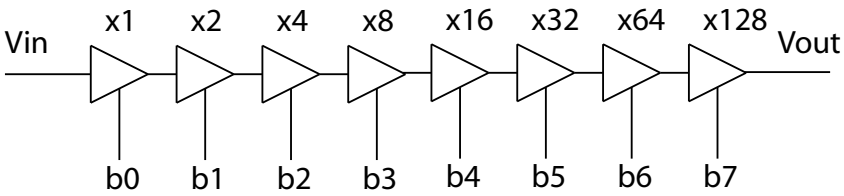

Figure 73: VCDL architecture for the proposed differential deskewing system.

of the system, N, and will be equal to $t_{min} \times 2^{N-1}$ where t_{min} is the minimum delay increment of the delay line. The maximum delay correction that can be achieved will be given by $t_{min} \times (2^N\text{-}1)$.

The VCDL in this proposal consists of a cascade of RC-delay blocks with the a digital control voltage applied instead of an analog control voltage. The schematic for each block is shown in Figure 15 [3, 21]. This block is simply an inverter followed by an adjustable load. If Vctrl is high, the gate capacitance from Mn2 is added to the signal path. If Vctrl is low, the gate of Mn2 is isolated from the rest of the circuit. By placing a large number of these blocks in series, the delay through the entire chain can be controlled.

For the eight-bit system proposed here, the delay is adjustable from 12.5 ps to 3.1875 ns in increments of 12.5 ps. To accomplish this, delay blocks corresponding to 12.5 ps, 25 ps, 50 ps, 100 ps, 200 ps, 400 ps, 800 ps, and 1.6 ns are built. These delays are the ideal design values. In practice, it is expected that the actual delays provided by any particular block will shift due to process, voltage, and temperature variation. As a result, the relative magnitudes of the delay blocks may not necessarily be exactly correct. Since the linearity of the delays provided by the entire VCDL is important, several modifications are made to ensure linearity across PVT variations.

The first modification is to ensure linearity of the larger delay blocks. To do this, delays greater than 50 ps are created by placing a number of 50 ps blocks in a cascade. The specific ratio of delays between any two blocks is set by the ratio of the number of 50 ps cells. If the delay of a 50 ps block shifts due to PVT variations,

it is expected that the delays of every 50 ps block will shift in a similar manner. This technique helps minimize the effects of broad shifts in process parameters on the relative magnitudes of the delay blocks. In addition, using a larger number of stages with each having a small delay results in smaller duty cycle variations than using a fewer number of stages with each having a large delay. The penalty for this implementation is an increase in the offset delay of the VCDL.

To further improve linearity and ensure monotonicity of delays, another improvement is made. The three lowest order bits are coded using thermometer encoding [36]. In a thermometer encoding, eight 12.5 ps blocks are created instead of the three blocks corresponding to the lowest three bits. The appropriate delays for the three bits are created by using the appropriate number of 12.5 ps blocks. This is illustrated in Figure 74. For example, for a delay of 25 ps, the last two blocks are used (Figure 74(a)). For a delay of 75 ps, the last six blocks are used (Figure 74(b)). Any particular delay is created by taking the next smaller delay and adding an additional 12.5 ps block. Since construction of any one delay requires use of the next smaller delay, the monotonicity of delays is guaranteed. In addition, since the larger delays are composed of a number of copies of smaller delays, the line displays greater linearity across PVT variations.

5.3 Experimental Results

The system has been fabricated in a TSMC 0.25μm, 1P5M process and tested using a 2.5 V power supply. For the test, a custom PCB was fabricated with traces having identical physical dimensions, but a difference in length of 2.1 inches to force a delay at the receiver. In practice, this delay difference can originate from process or load variations between the lines in addition to differences in trace length. Waveforms at both terminals of the terminating resistor are shown before (Figure 75) and after (Figure 76) correction. As evident in Figure 75, the delay difference between the traces

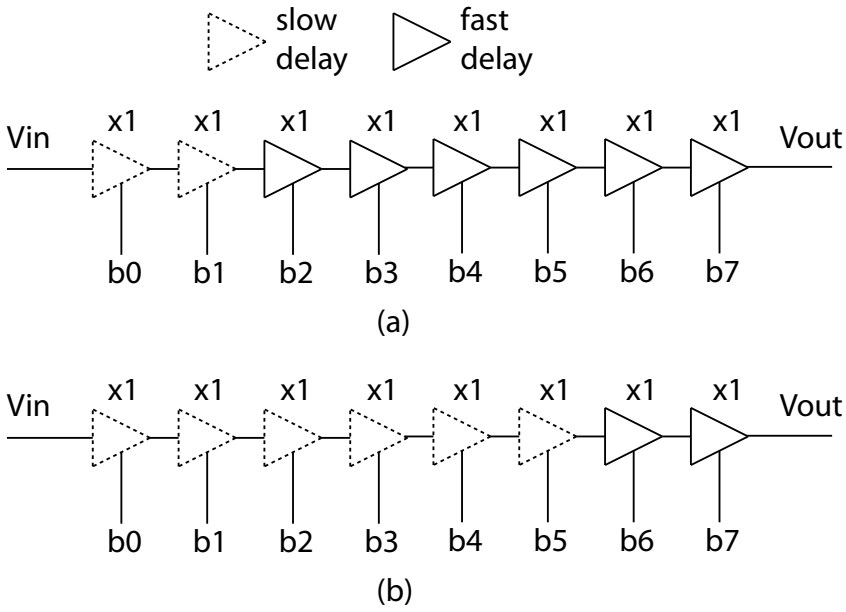

Figure 74: Illustration of thermometer encoding scheme.

causes a mismatch in the terminating resistor and ringing on both lines. Deskewing eliminates this ringing, resulting in a much cleaner signal across the terminating resistor, as shown in Figure 76. A die photo of the chip is shown in Figure 77. The core circuitry occupies 588μm$\times 235\mu$m, a third of which is consumed by the output drivers. The large size of the output drivers results from additional test circuitry incorporated to allow manual adjustment of the driver output impedance after fabrication. The system implemented for a single pair of differential lines consumes 100 mW of power.

5.4 Analysis and Characterization

A technique for deskewing differential PCB traces has been presented. This system implements a DLL using a precharge-type phase detector and a counter-controlled VCDL with a minimum resolution of 12.5ps. The system has been verified in simulation in a 0.25μm process and is found to eliminate skews of over 950 ps between traces.

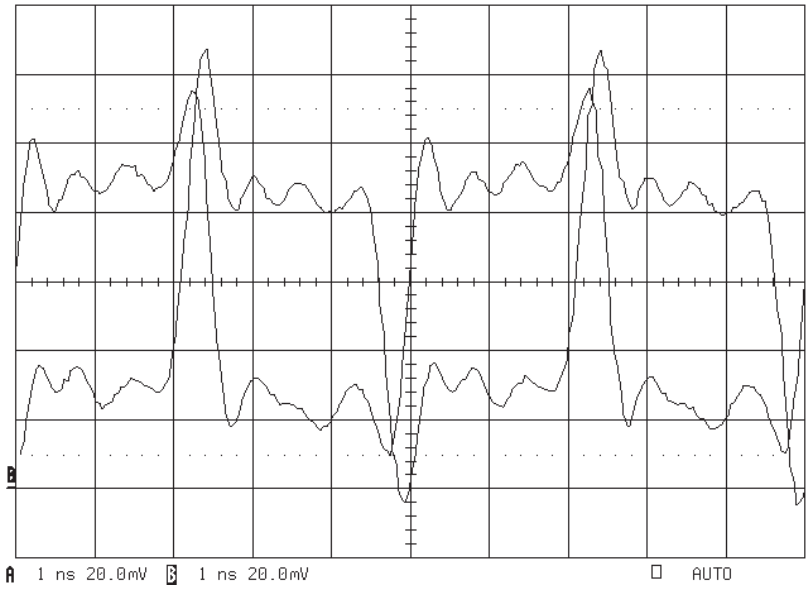

Figure 75: Waveforms at the receiver before deskewing.

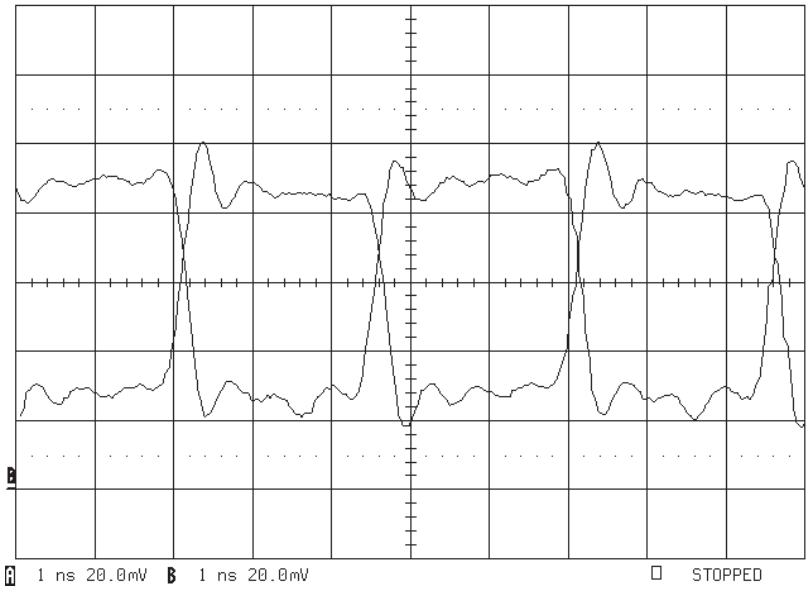

Figure 76: Waveforms at the receiver after deskewing.

5.4.1 Resolution

The resolution of a deskewing system is typically used to describe the accuracy with which the signals at the receiver are aligned. For a single-ended system, the waveforms at the receiver can all be compared at the same trip point (for example, $V_{dd}/2$). For a differential system, the positive and negative traces have difference DC offsets,

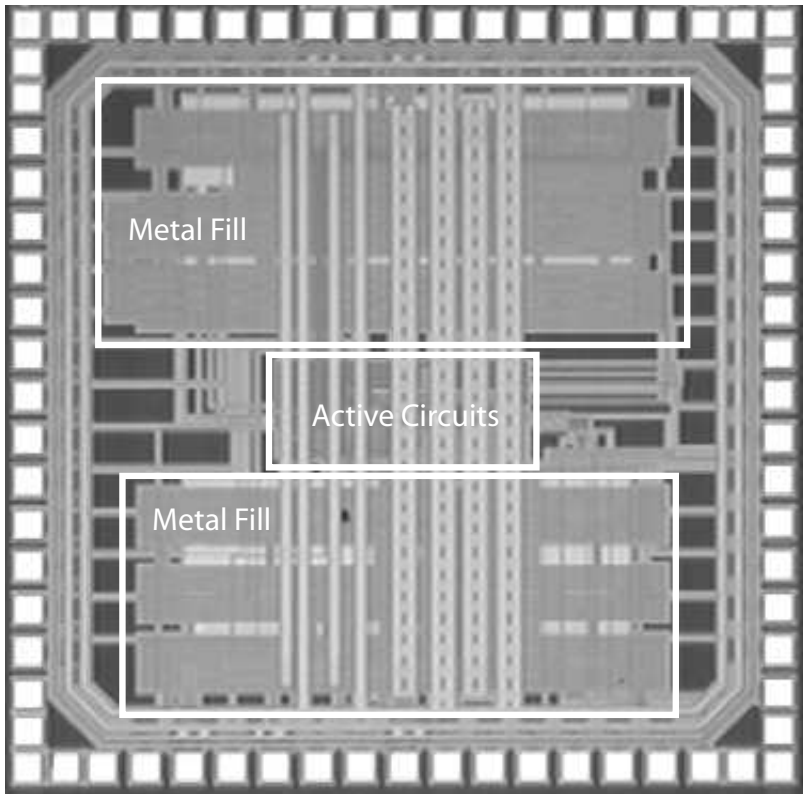

Figure 77: Die photo.

so this simple comparison will not work. To describe the resolution of the differential deskewing system, the alignment of the inputs to the phase comparator will be considered. In general, these are the signals whose phases are compared in the DLL. In addition, these signals are important because the basic functionality of the deskewing system is to align the phase comparator inputs, with the consequence, if appropriately designed, being the alignment of the signals at the receiver.

The simulated skew between the phase comparator inputs as the system achieves a lock is shown in Figure 78. For this simulation, the positive PCB trace is 50.8 mm in length and the negative PCB traces is 104.14 mm in length. This forces an initial skew between the bits of over 200 ps. In addition, the fixed DL for the negative PCB trace is programmed with an initial control word of 10000000 to allow for both

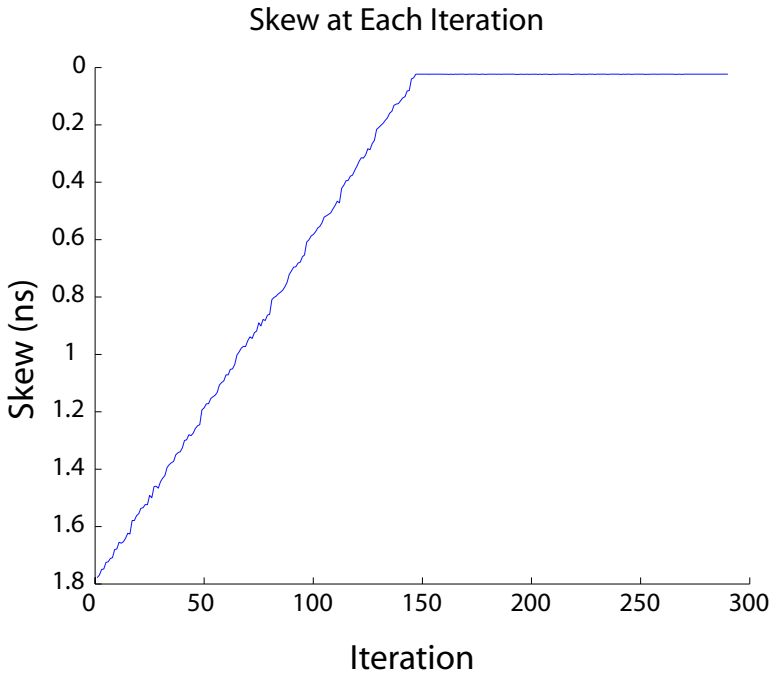

Figure 78: Skew between signals at the phase comparator input as the system converges to a lock.

positive and negative skew to be corrected. This control word injects an additional delay of 1.6 ns, bringing the total initial skew to approximately 1.8 ns. As the system achieves a lock, the skew is gradually reduced to approximately 20 ps. In simulation, this is the best resolution of the system and is set by the quantization factor of the VCDL. In addition, simulation noise causes the delay increments to be non-ideal, or not exactly equal to the design goal of 12.5 ps.

The resolution of the differential deskewing system described here is limited in two fundamental areas: skew detection and skew correction.

5.4.1.1 Skew Detection

The first limitation is the minimum skew between lines that can be detected. Provided that the detection circuits are identical, this is a limitation of the phase comparator. The precharge-type phase comparator in this implementation is found in simulation to have a resolution of approximately 12.5 ps. Use of a different phase comparator or

improvement of the current phase comparator could result in improved skew detection resolution.

5.4.1.2 Skew Correction

If the phase comparator has an arbitrarily fine resolution, the system resolution limitation will shift to the skew correction circuitry. The skew correction limitation will be determined by the VCDL. The VCDL in this implementation has a resolution of 12.5 ps and has been designed to match the resolution of the phase comparator. The RC-type delay stage will experience a shift away from the desired delay as PVT variations occur. However, the iterative nature of the DLL can compensate for these variations and always achieve a resolution equal to the quantization factor of the VCDL. A finer resolution could be achieved by appropriate design of another VCDL. Even though an arbitrarily small delay difference can be created in simulation, the smallest delay difference that could actually be fabricated will be limited by process variations.

5.4.2 Full Scale Range

The range of correction allowed by the system depends on the VCDL used. The eight-bit VCDL used in this implementation allows for a total deskewing range of 3.1875 ns. However, this range can only be achieved if the positive trace is longer than the negative trace and the fixed delay lines are set to minimum delay. In an application where it is unknown in advance which trace is the longest, then the fixed delay line must be set to some non-minimum delay to account for the possibility that the positive trace is the short trace. For the maximum total range, the fixed delay line will be set to 10000000, which is the middle value for the VCDL. In this case, the system can correct skews between -1.6 ns and +1.5875 ns. Extensions in range can be achieved by adding additional higher-order bits to the VCDL. This must be accompanied by a corresponding increase in the bit width of the counter used to

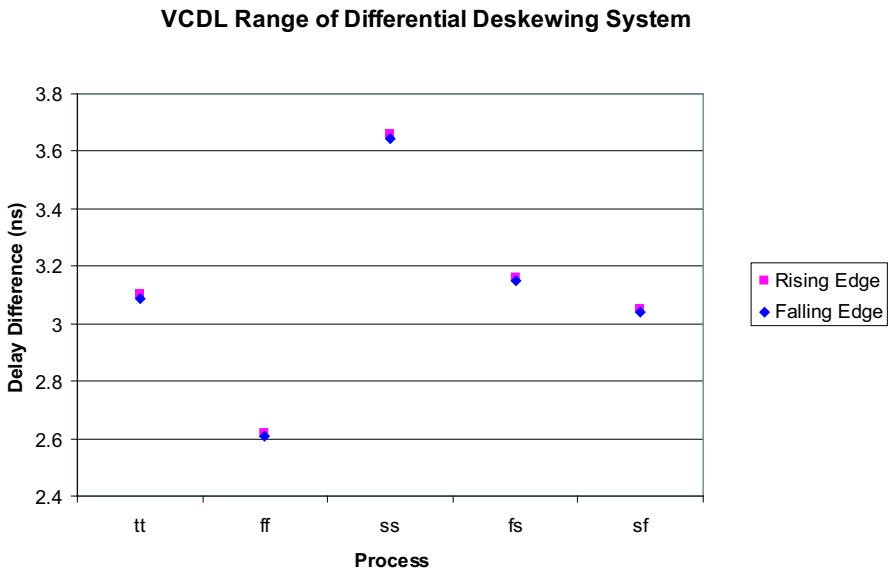

Figure 79: Simulated delay range of the VCDL for several process corners.

control the VCDL, although increasing the counter bit width is typically a trivial matter by comparison. The maximum delay difference that can be provided by the VCDL for several process corners is shown in Figure 79. As expected, the maximum delay difference that can be generated will depend on the process corner. In addition, temperature and power supply variations will also cause variations in the total delay differences. The simulated data indicates a very close correspondence between the delay differences for both the rising and falling edges.

5.4.3 Conversion Time

The conversion time for the differential deskewing system is fundamentally different than that for the open-loop deskewing system. Since the differential deskewing system is a DLL, a number of cycles will be required to achieve a lock. Therefore, two conversion times can be defined. The first time is the time required per iteration to make a phase comparison and then decide upon and set the counter state. This period will be referred to as the decision time, $T_{decision}$. The second time is the total time required to achieve a lock, T_{lock}. This will depend on both $T_{decision}$ and the number

of iterations required to achieve a lock, N_{lock}. The decision time will depend on the particular implementation chosen. For the system described here, this time will be

$$T_{decision} = T_{buf} + 2T_{PCB,positive} + T_{detect} + T_{VCDL} + T_{phase\,comparator} + T_{counter\,control} + T_{counter} \quad (100)$$

The total decision time includes the forward delay through the output buffer (T_{buf}), and PCB trace ($T_{PCB,positive}$). The remaining terms account for the return path and the control circuitry. The return path includes the delay of the reflection through the PCB trace along with the detector delay (T_{detect}) and a VCDL (T_{VCDL}). The control circuitry delay is composed of the delay through the phase comparator ($T_{phase\,comparator}$), counter control block ($T_{counter\,control}$), and the counter delay ($T_{counter}$). Simulated values for these various delays are shown in Table 7. As the table indicates, the conversion time in this implementation is dominated by the delay through the VCDL and the maximum round-trip delay through the PCB trace. The VCDL delay will depend on the control word being supplied to the line and can vary dramatically as the control word changes.

Table 7: Differential deskewing system conversion time breakdown.

Component	Delay
T_{buf}	620 ps
$T_{PCB,positive}$	1.83 ns
T_{detect}	310 ps
T_{VCDL}	5.5 ns
$T_{phase\,comparator}$	300 ps
$T_{counter\,control}$	1.5 ns
$T_{counter}$	1.0 ns
$T_{conversion}$	12.89 ns

The number of iterations required to achieve a lock depends on the initial skew between the traces and the quantization step of the VCDL. The total number of

iterations will be

$$N = \frac{T_{skew}}{t_{min}} \tag{101}$$

The total lock time can then be given by

$$T_{lock} = NT_{decision} = \frac{T_{skew}T_{decision}}{t_{min}} \tag{102}$$

Having a very small delay step will result in improved system deskewing accuracy, but will increase the lock time proportionally.

5.4.4 Delay Step Linearity

An important characteristic of any DLL is the linearity of the delay steps. Generally, this is a greater problem for an analog-controlled DLL, where the voltage to delay transfer function may not be perfectly linear. For a digitally controlled DLL, on the other hand, every delay step will ideally be of exactly the same size - this will correspond to the quantization factor of the line. Figure 80 shows simulated delays through the VCDL for all control words. As evident in the figure, the delay steps are very linear.

5.4.5 Delay

The delay through the signal path of the differential deskewing system is an important characteristic of the overall system. This delay will limit the maximum data rate that can be deskewed. Examination of Figure 66 reveals that the total delay through the differential deskewing system will be given by

$$T_{delay} = T_{offset,VCDL} + T_{program,VCDL} + T_{buf} \tag{103}$$

where $T_{offset,VCDL}$ is the offset delay of the VCDL, $T_{program,VCDL}$ is the additional delay correction that is programmed into the VCDL, and T_{buf} is the delay through the output buffer. Similarly to the open-loop deskewing system, the first two terms will be determined by the particular technique used for implementation of the VCDL.

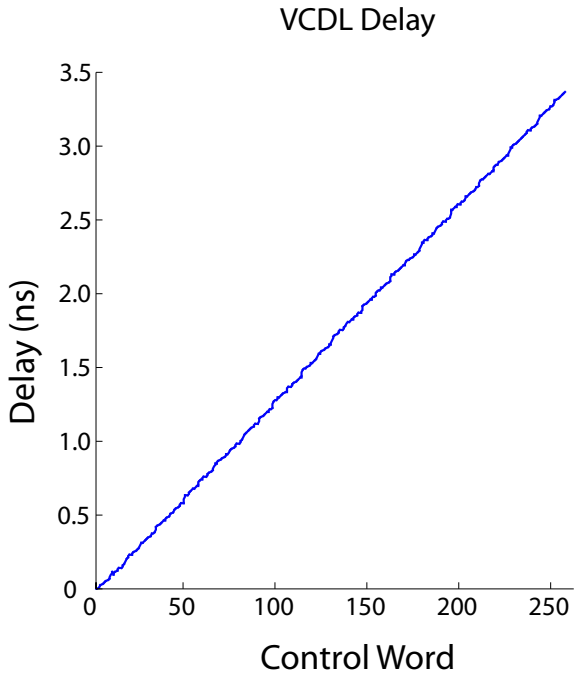

Figure 80: Simulated delays through the VCDL.

The third term will depend on the output buffer design. The minimum and maximum delays through the system are shown in Figure 81 and tabulated numerically in Table 8. The minimum delay is when the VCDL control word equals 00000000. The maximum delays is when the VCDL control word equals 11111111.

As evident in the figure, the rise and fall delays are nearly identical. This is due to the fact that the total delay through the system is dominated by the VCDL, which is composed of an even number of identical stages. Every edge propagating through the system will therefore experience the same number of rising and falling transitions. While each stage may have a different rise time and fall time, the total signal path includes the same number of rising and falling transitions for each edge that propagates through the system. Therefore, the total delay for each edge will be the same. The small differences that do exist are due to the unbalanced gates in the system, such as the multiplexor and the output buffer.

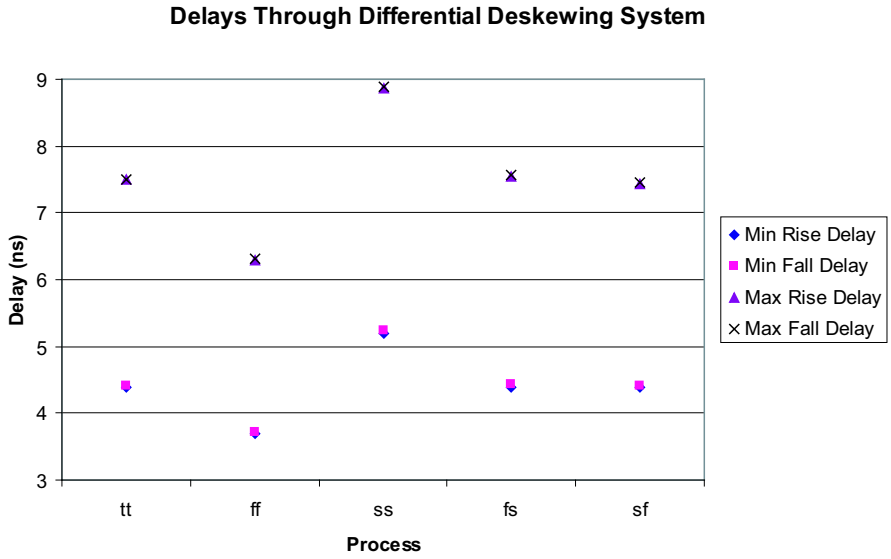

Figure 81: Simulated delays through the differential deskewing system for minimum (00000000) and maximum (11111111) values programmed into the VCDL.

Table 8: Delays through the differential deskewing system.

	Min Delay (00000000)		Max Delay (11111111)	
Process	Rise Delay (ns)	Fall Delay (ns)	Rise Delay (ns)	Fall Delay (ns)
tt	4.385	4.416	7.489	7.504
ff	3.683	3.711	6.301	6.318
ss	5.202	5.235	8.859	8.878
fs	4.394	4.426	7.555	7.573
sf	4.381	4.411	7.433	7.450

5.4.6 Maximum Data Rate

The maximum data rate through the differential deskewing system was determined in simulation and verified experimentally. Using the slowest process parameters, the system can support data rates up to 400 MHz for an input with a 20% duty cycle. Using an input with a 50% duty cycle, the maximum frequency is found to increase to 1 GHz. This is the data rate that can be supported after deskewing. While the system is being programmed, the maximum input frequency will be determined by the conversion time and will be approximately 75 MHz.

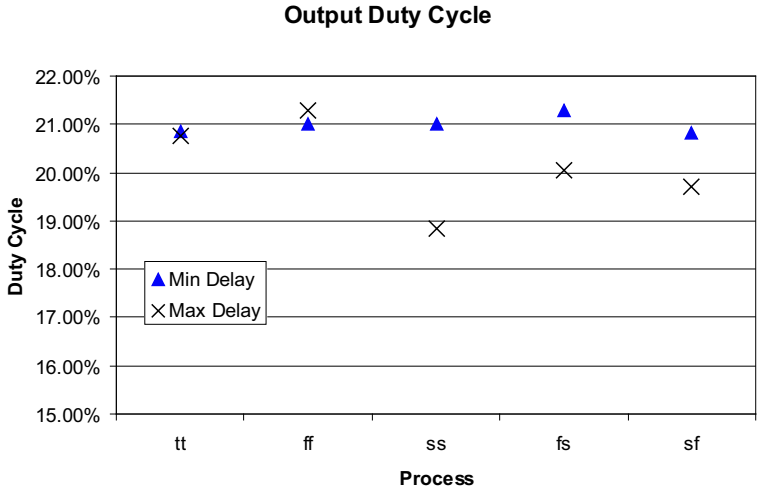

Figure 82: Simulated duty cycle at the output of the differential deskewing system for minimum (00000000) and maximum (11111111) values programmed into the VCDL when the input duty cycle is 50%.

5.4.7 Duty Cycle Distortion

The output duty cycle of the differential deskewing system for several process corners are shown in Figure 82. For the simulation, the input waveform has exactly 20% duty cycle and is run at a high frequency (400 MHz) in a typical process. Simulation results indicate a maximum duty cycle variation of 4.7%. This result is substantially better than that for the open-loop deskewing system. This is due to the fact that several steps were taken during the design of the VCDL for the differential deskewing system to specifically reduce any duty cycle distortion that may occur, as discussed in Section 5.2.3.

5.4.8 Noise Margin

For the differential deskewing system, the detector noise margins can be determined in much the same way as for the single-ended system. In the differential system, however, the magnitude of the reflected waveform will be only half the magnitude of

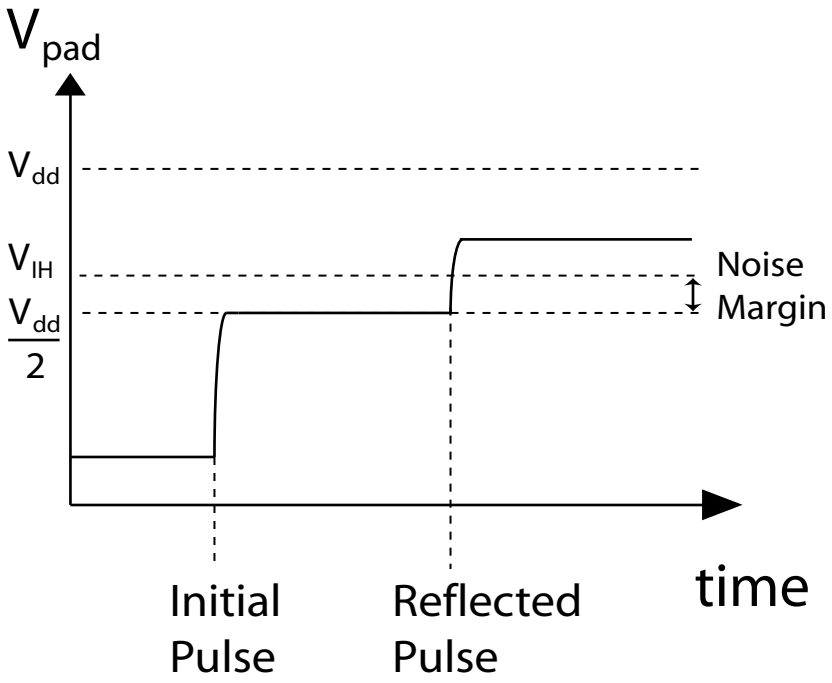

Figure 83: Illustration of reflection detector noise margins for a differential system.

the transmitted waveform, as illustrated in Figure 83. If V_{IH} is given by

$$V_{IH} = \frac{V_{dd}}{2} + \frac{3V_{dd}/4 - V_{dd}/2}{2} = \frac{5V_{dd}}{8} \tag{104}$$

The noise margin will then be given by

$$V_{NM} = \frac{5V_{dd}}{8} - \frac{V_{dd}}{2} = \frac{V_{dd}}{8} \tag{105}$$

Comparison to Equation 21 for the open-loop system indicates that the differential deskewing system has only half the noise margin of the open-loop system. This means that error sources such as overshoot, offsets in the comparator, and variations in the power supply voltage are more likely to create false switches at the detectors.

CHAPTER VI

A CURRENT-BASED DESKEWING SYSTEM

6.1 A Current-Based Deskewing System

Traditionally, deskewing systems utilizing time-domain reflectometry have focused exclusively on the transmission and reflection of voltage waves. This is due, in part, to the ease with which a voltage pulse can be created and a reflection detected. Voltage pulse reflections can be detected on-chip using a simple Schmitt trigger circuit or a comparator. The voltage waveform carries information about the propagation delay through the line and the relative impedances of the line and driver. Whenever a voltage pulse is created, however, a corresponding current pulse through the driver is also created. The current waveform carries sufficient information about the line and driver to allow for data bus deskewing and should not be neglected. This chapter presents an architecture that achieves data bus deskewing by examination of the current pulses through the output drivers. Use of current information instead of voltage information provides several distinct advantages, as discussed at the end of this chapter.

6.1.1 Characteristics of Current Pulses

For illustration of the basic principles, consider a system consisting of a matched driver and line and open-circuited at the receiver. This basic setup is illustrated in Figure 84. When the line is pulsed by a voltage step at the source at time $t = 0$, the

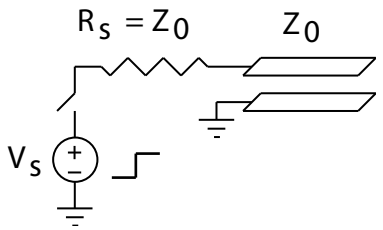

Figure 84: Basic setup to illustrate current pulses through the driver.

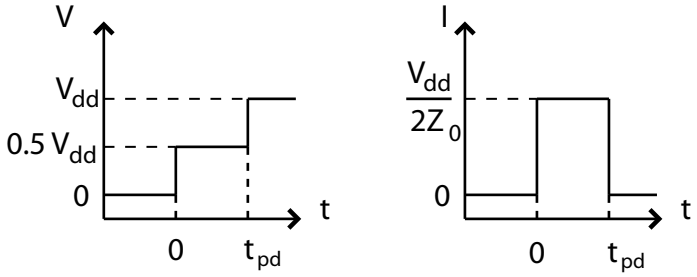

Figure 85: Voltage and Current Waveforms at the Source

current through the driver will be given by

$$I(0) = \begin{cases} 0 & \text{for } t < 0 \\ \frac{V_0^+}{2Z_0} & \text{for } 0 < t < 2t_{pd} \\ 0 & \text{for } t > 2t_{pd} \end{cases} \tag{106}$$

where t_{pd} is the propagation delay through the line.

The voltage and current waveforms at the chip are illustrated graphically in Figure 85 for an idealized system as shown where $R_S = Z_0$. In general, as the voltage at the source end of the line steps up to a constant value, the current also steps to a constant value. The magnitude of the current pulse through the driver will be related to the voltage at the driver output by the driver impedance, according to Ohm's Law. The width of this current pulse is directly proportional to the delay through the line.

6.1.2 Use of Current Pulses

To detect voltage reflections on lines, a simple level sensitive detector is used. The current based system, however, takes a new approach. The current pulse through the driver is measured and the signal is used to charge a capacitor. This provides a

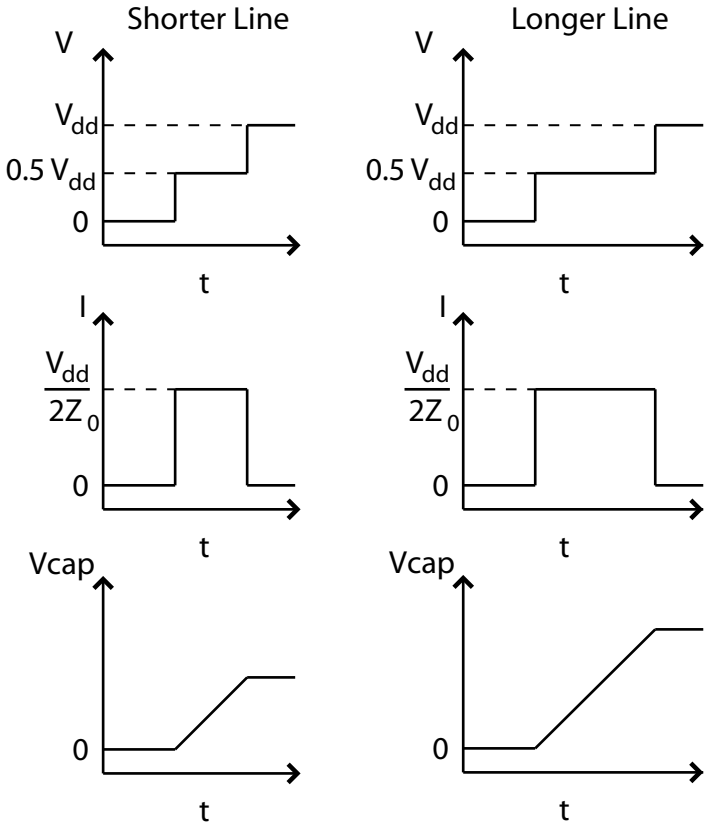

Figure 86: Voltage and current pulses for two lines of different lengths. The longer line provides a greater charge to its corresponding capacitor.

final charge on the capacitor that is an integration of the current signal. Since the width of the current pulse is proportional to the length of the PCB trace, the final voltage on the capacitor will also be proportional to the length of the PCB trace. If this approach is used for two lines of dissimilar lengths, then the capacitor with the higher voltage will correspond to the line with the longer length. This is illustrated in Figure 86. To actually make use of this information, a comparator is used to compare the voltages on the capacitors for each line. The comparator output will indicate which capacitor has a greater charge.

6.1.3 A Current-Based Deskewing Architecture

A voltage-based deskewing system operates in a purely switched manner - voltage reflections cause a switch at the detectors, which propagates back through the system.

A current-based deskewing system operates on a fundamentally different principle than the voltage-based systems. The current-based system compares the width of the current pulses through the output drivers. Therefore, an entirely new architecture will be required. A simple implementation is shown in Figure 87. For illustration in this schematic, an idealized driver is used to drive the off-chip PCB trace. The voltage drop across the driver impedance indicates the current through the driver. The specific technique used to sense the current through the driver will depend on the particular driver used.

On each iteration, a pulse is simultaneously written to each of the *DataN* inputs. The current signal through the output driver during the rising transition is used to charge the capacitor for each line. The capacitor voltages are compared and the delay through each line is adjusted until that line's capacitor voltage matches the reference line's capacitor voltage. Before each iteration, the capacitors are precharged to a DC value. If both current signals are integrated from beginning to end, however, every comparison will yield the same result - the longer line will always have a greater voltage on its corresponding capacitor. To allow for a comparison that accounts for any marginal corrections that may have already been applied, the integration for any particular line does not begin until both current pulses have begun. The pulse for each line will be shifted until the trailing edge is aligned with the reference line's trailing edge. Figure 88 illustrates the effect of a small shift on the final capacitor voltage. A simple 4-iteration example showing the alignment of two waveforms is shown in Figure 89. In practice, the waveform shifts in steps equal to twice the quantization factor of the VCDL and will require many cycles to converge to a final solution. Alignment of the trailing edges of the current waveforms indicates alignment of the reflected waveforms at the transmitting chip. If there exists a one-way propagation delay difference of t_d between a given line and the reference line, then that line will have been corrected to $2t_d$ to account for the round-trip delay. For programming,

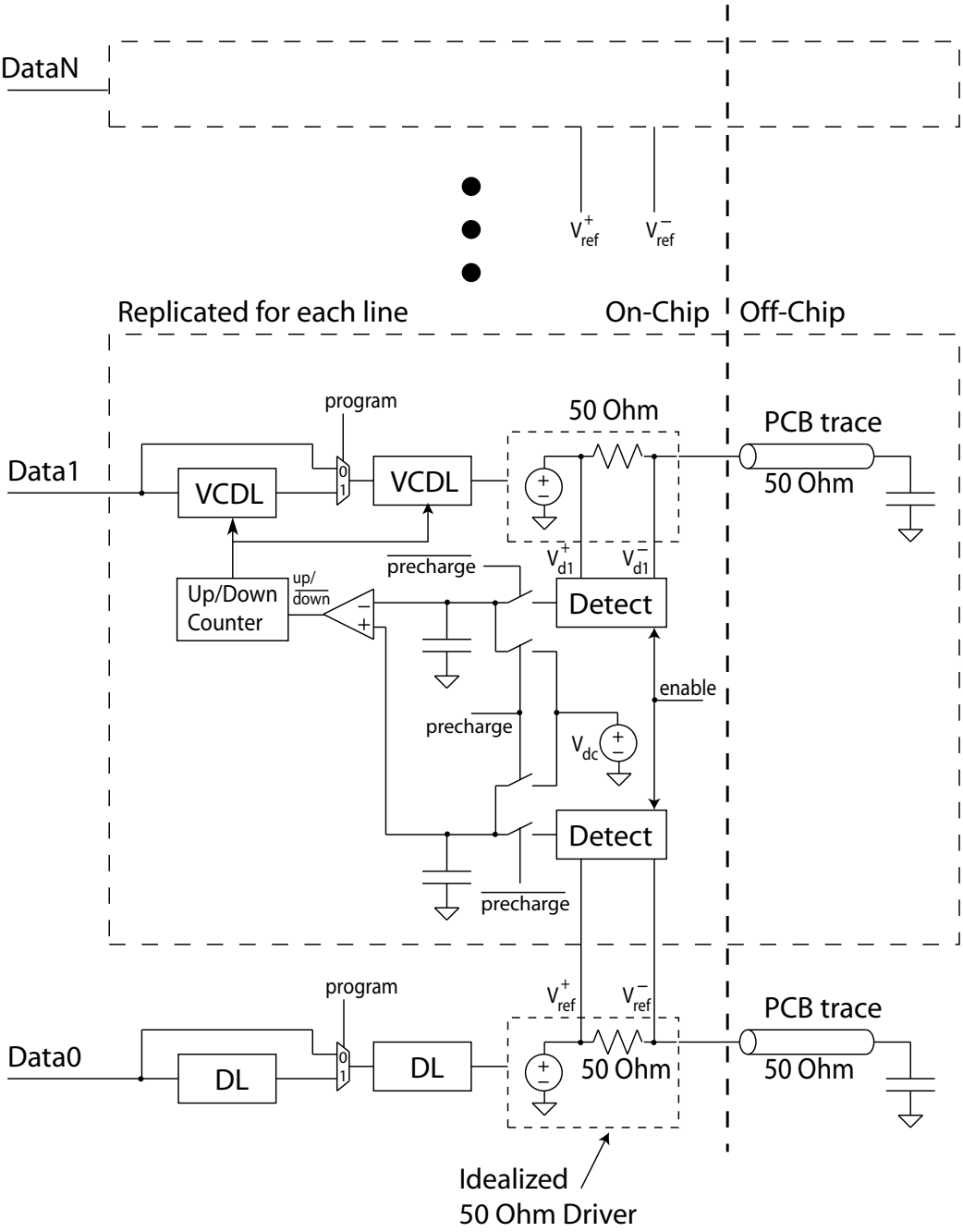

Figure 87: Current-based deskewing architecture.

two VCDL's are placed in series in the data path. Removing one of the VCDL's after programming reduces the delay correction to t_d, thereby aligning the signals at the receiver.

The final voltage on a capacitor when being charged by a constant current, I_{DC},

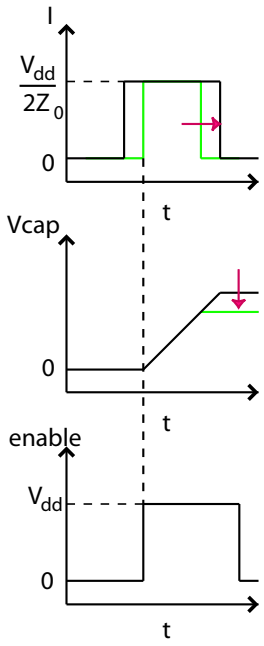

Figure 88: Illustration of marginal correction in a current-based deskewing system.

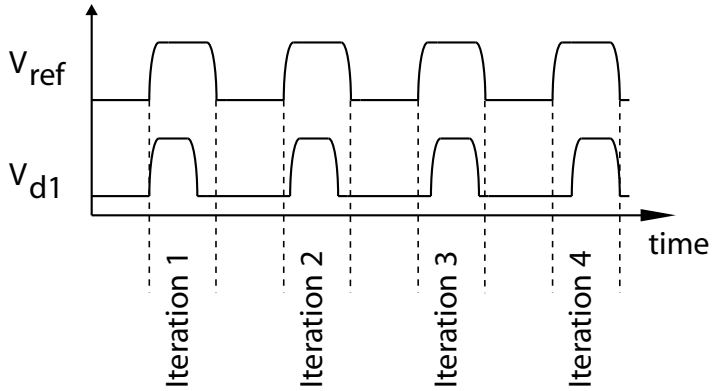

Figure 89: Illustration of waveform convergence in a current-based deskewing system.

will be given by

$$V_{final} = \frac{Q_{total}}{C} = \frac{I_{DC} t_{total}}{C} \tag{107}$$

In this equation, t_{total} is the total time the capacitor is charging. It is assumed that all capacitors are charged with the same I_{DC} and have the same capacitance value. For the reference line capacitor in the N^{th} bit, the total charging time will be

$$t_{total,ref} = 2t_{d,ref} - 2t_{VCDL,N} \tag{108}$$

where $t_{VCDL,N}$ is the delay programmed into the VCDL for the N^{th} line and $t_{d,ref}$ is the propagation delay through the reference line.. The line's charging time will be given by

$$t_{total,N} = 2t_{d,N} \tag{109}$$

The system will converge to a final solution when the charging times for the reference and the line capacitors are identical. At this point,

$$2t_{d,ref} - 2t_{VCDL,N} = 2t_{d,N} \tag{110}$$

Therefore,

$$2t_{VCDL,N} = 2t_{d,ref} - 2t_{d,N} \tag{111}$$

Finally,

$$t_{VCDL,N} = t_{d,ref} - t_{d,N} \tag{112}$$

It can now be seen that the VCDL has been programmed to provide a delay that is equal to the propagation delay difference between the reference line and the N^{th} line. If the reference line is not the longest line, the same equations will apply, except $t_{VCDL,N}$ will be a negative number (i.e., the N^{th} VCDL provides less delay than the VCDL in the reference bit).

6.2 Implementation Details

6.2.1 Output Drivers

The driver circuit shown in Figure 90 allows the system to drive a matched 50 Ω line and provides the necessary current information. The voltage drop across the 25 Ω resistors indicates the current through the driver on the rising (R_p) or falling (R_n) transition. The transistors are sized to give equivalent 25 Ω impedances while driving the PCB trace.

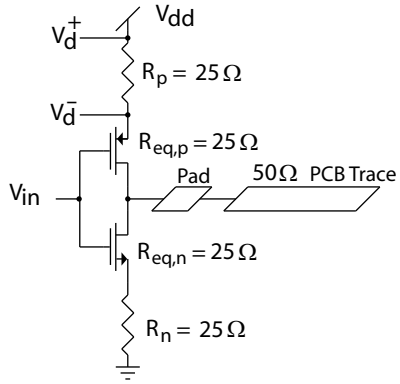

Figure 90: Output driver used in the current-based deskewing system.

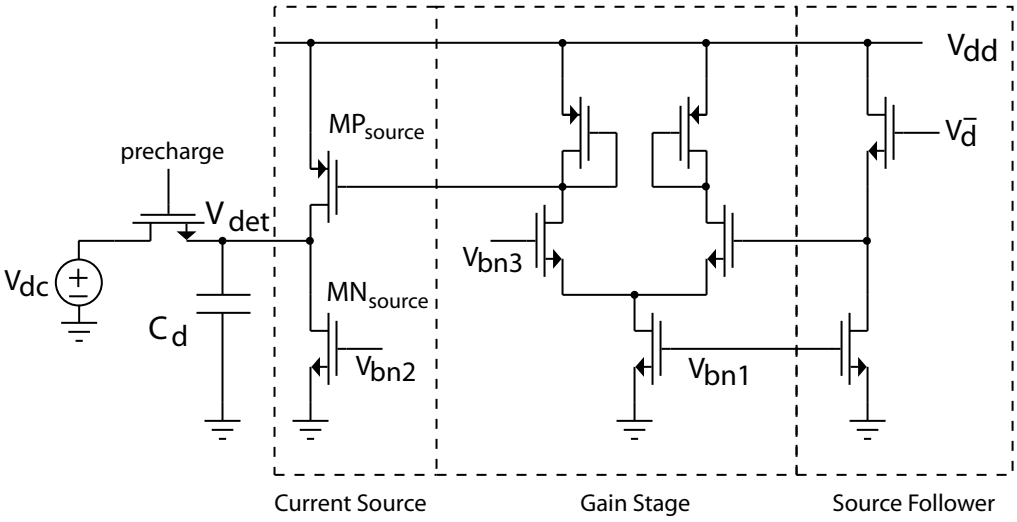

Figure 91: Current detection circuitry.

6.2.2 Current Detectors

To test the current-based architecture, a simple current detector scheme is used. The basic circuit is shown in Figure 91. In this circuit, V_{bn1}, V_{bn2}, V_{bn3}, and V_{dc} are all external DC biases provided to the circuit. In addition, the *precharge* signal is also generated externally. The signal V_d^- is the voltage drop across the series resistor in the output driver (see Figure 90). The detector circuitry is simply a source-follower followed by a gain stage. The gain stage in this implementation is a low-gain amplifier and provides a gain of only 1.6 dB. The resulting signal is used to control a current sourcing device, MP_{source}. When the output driver is not sourcing any current (i.e.

$V_{det}^{-} = V_{dd}$), the current source devices MP_{source} and MN_{source} are sized and biased to provide identical current when $V_d = V_{dc}$ such that the total charge on the decision capacitor C_d does not change.

6.2.3 Voltage Controlled Delay Line

For verification in simulation, the VCDL from the differential deskewing system was used in the current-based deskewing system. This 8-bit VCDL incorporates several design features to ensure linearity and monotonicity across PVT variations and has been verified both in simulation and experimentally. A more detailed discussion was given in Section 5.2.3.

6.2.4 Simulation Results

Final verification of the system was performed in simulation in a 0.25 μm process for an eight-line system. For testing, line lengths of 3.0, 3.9, 4.9, 5.9, 6.9, 7.1, 8.8, and 9.9 inches were used. Simulation results are shown in Figure 92 before and after deskewing for a typical process at room temperature. Before correction, the maximum length difference of 6.9 inches creates a skew at the receiver of nearly 1.2 ns. After correction, maximum skew between lines has been reduced to 35 ps.

6.3 Analysis

6.3.1 Resolution

The fundamental system resolution limitation of the system will lie in one of two areas: skew detection and skew correction.

6.3.1.1 Skew Detection

This system detects skew between traces by comparing the final voltages on two capacitors. The measurement resolution will therefore be limited by the minimum voltage difference that can be detected. If the capacitors are charged using a constant

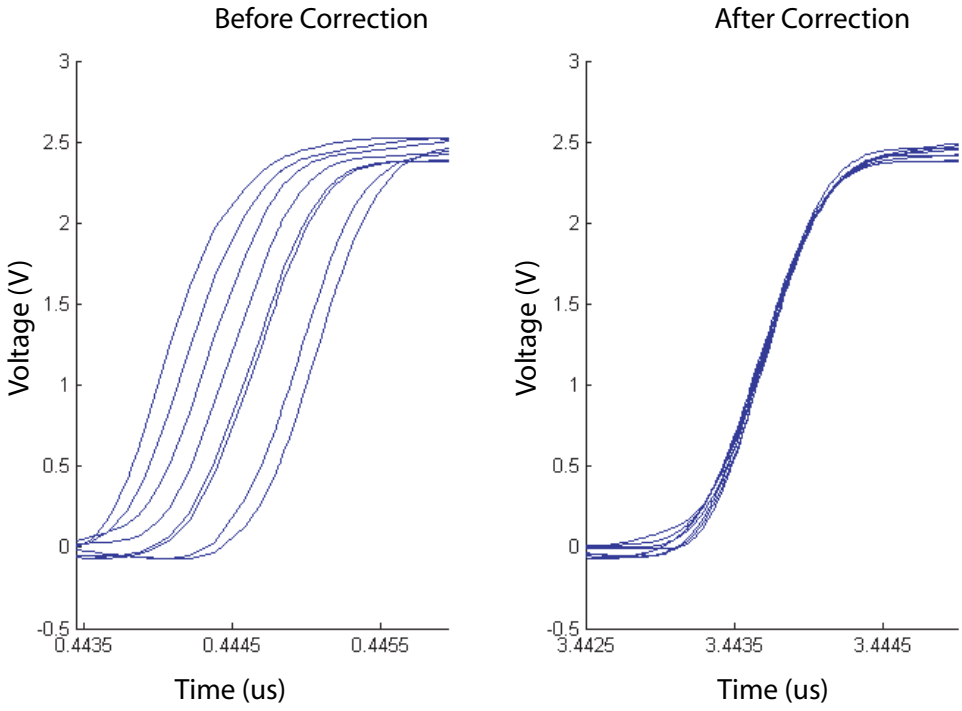

Figure 92: Simulated waveforms at the receiver for an eight-line system before and after correction.

current of I_{DC} and have a capacitance of C_d and the comparators have a resolution of V_{min}, then the minimum capacitor charge difference that can be detected will be given by

$$\Delta Q_{min} = V_{min} C_d \tag{113}$$

The difference in charge between the capacitors will also be given by

$$\Delta Q_{min} = I_{DC} t_{min} \tag{114}$$

Therefore, the minimum time difference that can be measured, t_{min}, will be given by

$$t_{min} = \frac{V_{min} C_d}{I_{DC}} \tag{115}$$

Using typical values of $V_{min} = 5\,mV$, $C_d = 1\,pF$, and $I_{DC} = 1\,mA$ gives a minimum resolution of $t_{min} = 5\,ps$. This resolution can easily be improved by increasing I_{DC}, improving the comparator resolution, or adjusting the capacitor values.

6.3.1.2 Skew Correction

If the system can detect an arbitrarily small skew by appropriate choice of capacitors, comparators, and charging current, then the system resolution limitation shifts to the delay correction circuitry, the VCDL. In this implementation, two digitally-controlled VCDL's are cascaded in the data path during programming. Therefore, the minimum delay correction during programming will be equal to twice the quantization factor of the VCDL. However, during programming twice the actual skew is corrected. After programming, the correction is reduced by half, allowing for a correction equal to the quantization factor of the VCDL. Thus, the minimum resolution achievable will be equal to the minimum resolution of the VCDL (or the quantization factor for a digitally-controlled VCDL). Use of the VCDL from Section 5.2.3 provides a minimum delay correction of approximately 12.5 ps. An analog-controlled VCDL or a different digitally-controlled VCDL could be used to improve the system resolution beyond 12.5 ps.

6.3.2 Delay

As evident in Figure 87, the total delay through the deskewing system during normal operation (not programming) will be given by

$$T_{delay} = T_{offset,VCDL} + T_{program,VCDL} + T_{mux} + T_{buf} \tag{116}$$

which consists of the offset delay of the VCDL ($T_{offset,VCDL}$), the additional delay correction programmed into the VCDL ($T_{program,VCDL}$), the delay through a one-bit one-input multiplexor (T_{mux}), and the output buffer delay (T_{buf}). In general, T_{mux} will be less than two gate delays and will be relatively small. Appropriate design of the VCDL can reduce $T_{offset,VCDL}$ to an acceptably small amount. This leaves the major contributors of the delay to be the output buffer, which is present in any design, and the delay correction. Therefore, the overall impact of the deskewing system to a given system delay can be made to be quite small.

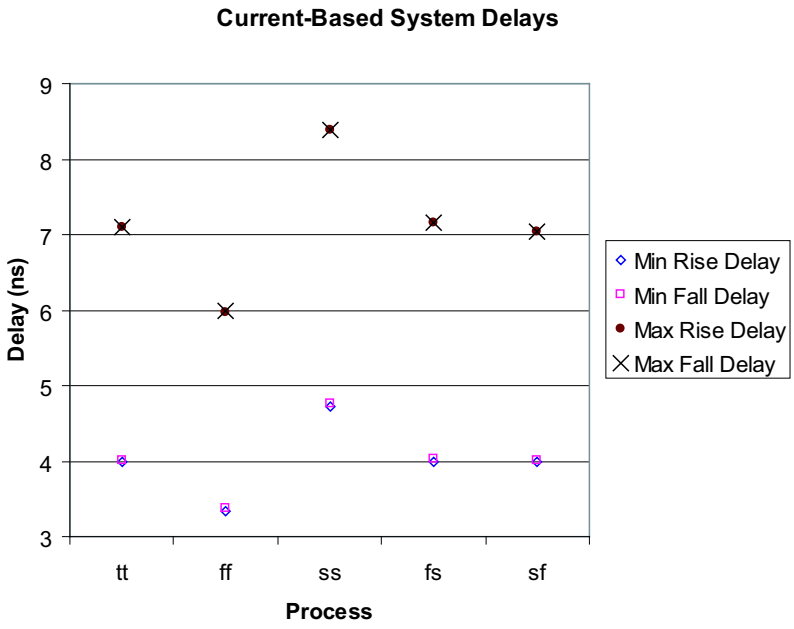

Figure 93: Simulated delays through the current-based deskewing system for minimum (00000000) and maximum (11111111) delays programmed into the VCDL.

The minimum and maximum delays through the system are shown in Figure 93 and tabulated numerically in Table 9. The minimum delay is when the VCDL control word equals 00000000. The maximum delay is when the VCDL control word equals 11111111.

Table 9: Current-Based System Delays

	Min Delay		Max Delay	
Process	Rise Delay (ns)	Fall Delay (ns)	Rise Delay (ns)	Fall Delay (ns)
tt	3.984	4.018	7.090	7.101
ff	3.346	3.376	5.966	5.982
ss	4.724	4.760	8.387	8.392
fs	3.993	4.026	7.154	7.168
sf	3.981	4.014	7.035	7.043

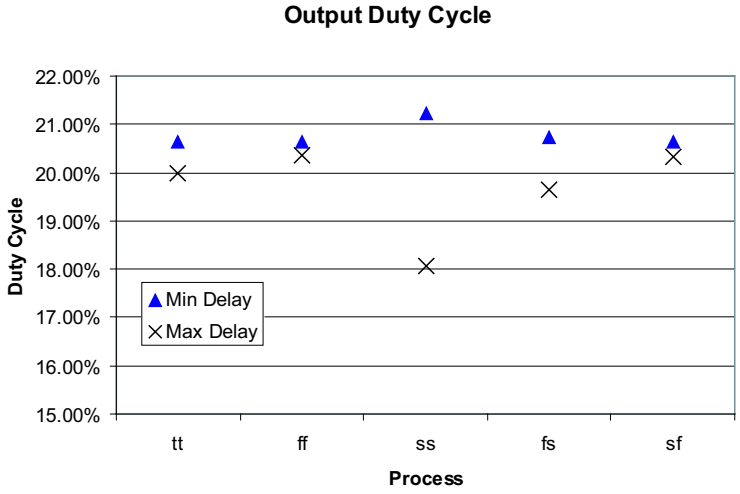

Figure 94: Simulated duty cycle at the output of the current-based deskewing system for minimum (00000000) and maximum (11111111) delays programmed into the VCDL when the input duty cycle is 50%.

6.3.3 Maximum Data Rate

Simulation was performed to determine the maximum data rate sustainable by the current-based deskewing system. Using the slowest process parameters, the maximum data rate is found to be 350 MHz.

6.3.4 Duty Cycle Distortion

The output duty cycle of the differential deskewing system for several process corners is shown in Figure 94. For the simulation, the input waveform has exactly 20% duty cycle and is run at a high frequency (350 MHz). Simulation results indicate a maximum duty cycle variation of 4.6%. This result is quite good, due to the steps taken during the design of the VCDL to reduce duty-cycle distortion, as discussed in Section 5.2.3.

6.3.5 Power Supply

The current-based deskewing system has been implemented predominantly using standard circuitry. The magnitude of the current signal will be given by Equation 106.

According to this equation, the current pulse will be proportional to the power supply voltage. However, the effect of scaling down the current pulse can easily be compensated by appropriately scaling the decision capacitors (C_d) or increasing the gain of the gain stage.

Voltage-based systems utilizing a switched reflection detector exhibit increased susceptibility to false switch at low supply voltages. This is due to the fact that the system noise margins scale directly with V_{dd}. The current-based system, on the other hand, does not rely on a switched detector. Therefore, there is no possibility of false switching resulting from reduced noise margins.

6.4 Advantages of Current Pulses

The current-based deskewing system has several advantages over the voltage-based systems. These advantages relate primarily to system-PCB trace interactions. In particular, the current-based deskewing system is relatively insensitive to several effects that create substantial problems for a voltage-based system.

6.4.1 Overshoot

The first major advantage of the current-based system is insensitivity to overshoot. Future systems are expected to have higher signal edge rates and lower supply voltages, making overshoot resulting from package parasitics an increasingly critical problem. Since the voltage-based systems rely on full switching of a detector, excessive overshoot that causes a false switch can completely block system operation. The current-based system, on the other hand, relies upon an integration of the current waveform through the driver. Overshoot at the output node appears as a peak in the current signal. This cannot cause any false switching in the current-based system. While it is possible that the peaking can introduce small errors into the final skew compensation, basic operation of the system will not be prevented. Therefore, the current-based system is more suitable for low-voltage applications where package

parasitics cause substantial overshoot at the chip outputs.

6.4.2 Driver and Trace Impedance Mismatch

Another major advantage of the current-based deskewing system is insensitivity to driver and trace impedance mismatch. In a voltage-based system, mismatches in driver and trace impedances cause shifts in the magnitude of the transmitted waves. These shifts can cause false switches in the reflection detectors or may make the detectors not sense the reflected waveforms.

In the current-based system, however, the trace propagation delay comparison is performed by integrating the current waveform through the driver. Mismatches between the driver and trace impedances will cause the magnitude of the driver current level to shift. However, if every driver is matched to each other and every trace is matched to each other, the current levels through each driver will be of the same magnitude. Therefore, an integration of the current signals will still give an appropriate measure of the relative propagation delays through the traces.

6.4.3 Dispersion

In the voltage-based deskewing system, dispersion combined with random variation in device threshold voltages created an error in the measured trace delay (Section 4.3.1). The current-based system is immune to errors resulting from dispersion effects. If every trace is of similar dimensions, then each will exhibit the same dispersion. Therefore, the edge rate of every reflected signal will be identical. When the current signals are then integrated, the trailing edge will be identical for every line and the effects of dispersion will be cancelled out.

6.5 Disadvantages of Current Pulses

Even though the current-based system has several advantages over voltage based systems, the current-based system also has several disadvantages.

6.5.1 Device Mismatch

The greatest disadvantage is susceptibility to device mismatch. The voltage-based systems are relatively insensitive to random mismatch between devices. Variations in threshold voltage between devices can introduce a delay difference in the reflection detection. However, this error will typically be quite small and can easily be reduced by correctly sizing the appropriate devices. This is the only area of the voltage-based system where threshold voltage mismatches between devices introduce significant error.

In the current-based system, however, matching of numerous devices is critical. Particularly, it is assumed that the output driver transistors and series resistors (Figure 90), detection circuits (Figure 91), all capacitors, and all current sources are identical for every line. Due to the large number of matched devices, more error will be introduced due to variations between devices. These variations may be due to localized heating, implant variations, or variations during etching and will cause every device in the system to be slightly different. These between-device variations can introduce error in several ways, as discussed below.

6.5.1.1 Capacitor Mismatch

One major area where device mismatch may introduce error is the measurement capacitors, C_d. If every capacitor is charged with an identical current, it is expected that the final voltage on the capacitors will indicate the relative lengths of the PCB traces. This assumes, however, that every capacitor has an identical capacitance. This will, in general, not be the case. PVT variations will cause mismatch between the capacitors. When charged with an identical current for the same period of time, the capacitor with a lower capacitance will have a lower final voltage than the capacitor with a higher capacitance. Therefore, mismatch between capacitors will make resolution of very fine delay differences impossible, presenting another fundamental limitation to

skew measurement. Ultimately, capacitor matching can be improved in layout by use of common-centroid techniques, but perfect matching cannot be achieved.

It is, in principle, possible to measure the capacitance of every capacitor and automatically adjust for any variations that may exist. This could be done, for example, by charging every capacitor using an identical current for the same length of time and then comparing the final voltages. The differences in the final voltages would indicate the degree of mismatch between the capacitors and the amount of compensation that would then be required to correct the mismatch errors. Further investigation of automatic compensation techniques is left as an area for future research.

6.5.1.2 Detection Circuitry Mismatch

Another potential source of error due to device mismatch is in the current detection circuit (Figure 91). If the gain of the gain stage or source follower for a particular line has more gain than for the other lines, that line will appear to be longer than the other lines. This will result in a delay offset for that line after programming.

Another error is injected if the bias currents between MP_{source} and MN_{source} are unequal. Any dc current bias difference between these devices will be added to the current generated by the detection signal, resulting in an offset voltage being added or subtracted from the final capacitor voltage. This in turn will also lead to a delay offset in the final skew correction.

CHAPTER VII

CONCLUSION AND FUTURE WORK

This concluding chapter presents a brief summary of the work presented in this dissertation. This is followed by a discussion of possible applications, a highlighting of the contributions made by the work, and a brief discussion of potential areas of future research.

7.1 Summary

This dissertation presented a study of deskewing systems in standard CMOS technologies. Examination of the previous techniques for signal deskewing led to the development of several new architectures. The architecture addressed several critical issues associated with signal deskewing in modern systems, such as deskewing wide data buses and differential signal transmission.

The first architecture presented was an open-loop deskewing system. This architecture could deskew a wide data bus in a single program cycle. Details of one possible implementation of this architecture were presented and validated through experimental measurement in a 0.25 μm process. The system was characterized with respect to delay, duty cycle distortion, conversion time, resolution, and noise margins. In addition, a detail investigation into overshoot effects resulting from parasitic package inductance was performed, resulting in a simple expression for approximating the magnitude of overshoot in a system. The magnitude of the overshoot is found to be proportional to the power supply voltage and parasitic inductance and inversely proportional to the signal rise time, implying that overshoot will become in increasingly challenging problem for systems utilizing voltage-based TDR techniques. Finally, the

effects of capacitive terminations on the system were examined and an analytical expression for predicting the effects was presented. The open-loop system was shown to effectively eliminate the effects of disparate loading on the PCB traces.

This was followed by a discussion of the performance limitations of the open-loop system, including delay measurement and correction. The design tradeoffs involved in choosing an oscillator for use in the system were discussed in terms of area consumed and minimum resolution. In addition, the effect of mutual inductance between the PCB traces was considered and its impact on system performance was examined along with the effects of dispersion on the system.

The second architecture presented was used to deskew a pair of PCB traces carrying a differential signal. An implementation of this system was also presented, along with experimental measurement validating the architecture in a 0.25 μm process. This system was also thoroughly characterized with respect to delay, duty cycle distortion, conversion time, resolution, and noise margins.

The final architecture presented utilized the current signal through the output drivers to deskew a wide data bus. This system was proposed to overcome some of the limitations of voltage-based designs. An implementation of the current-based architecture was presented and characterized. Validation was performed using simulation and a comparison with voltage-based designs was presented. The current-based system is found to have greater immunity to overshoot, dispersion, and driver/trace impedance mismatch than the voltage-based systems.

7.2 Comparison to Previous Techniques

In the past, several different techniques have been proposed to handle the problem of signal deskewing. The systems all utilized a DLL for skew correction. A summary of previous results is shown in Table 10. As compared to previous results, this work produces skew correction at a precision exceeding that of published techniques for

closed-loop systems. The open-loop system, while have a resolution somewhat worse than that of the best published results, has the advantage of short programming time and direct application to wide data busses. In addition, only the technique presented in [1] does not require the use of any replica delay lines for estimating off-chip propagation delays.

Table 10: Summary of previous deskew system results.

Source	Process	Resolution
[21]	0.6 μm	300 ps
[39]	0.75 μm	750 ps
[17]	2.0 μm	400 ps
[34]	0.5 μm	30 ps
[7]	0.25 μm	250 ps
[3]	0.8 μm	40 ps
[41]	0.35 μm	191 ps
[1]	0.8 μm	600 ps
This work (Open Loop)	0.25 μm	100 ps
This work (Differential)	0.25 μm	12.5 ps
This work (Current Based)	0.25 μm	35 ps

7.3 Applications

One of the motivating factors for this work was the universal nature of its applications. Any system that involves synchronous signal transmission across a PCB will be subject to signal skew. Deskewing techniques can be utilized in any of these applications. The systems presented have only a minimal impact on the original signal path and require few other resources from the chip - only the VCDL delay is added to the datapath and additional power is consumed only by the VCDL during normal operation. The remain circuitry consume power only while programming and can be turned off after programming has been completed.

An example application is a clock buffer chip on a motherboard. This chip may be required to transmit a clock signal to several target chips with identical phase at

high frequency. The target chips may be audio or video processors, memory modules, or bus interfaces. Each of the chips will be on a different part of the board, making it impossible to guarantee that every trace would be perfectly matched. Use of a deskewing system in this application would eliminate the skew at the receivers. No additional steps would be required during the PCB design or in the design of the receiver chips.

Another application is on the data bus between a processor and an external memory module. This bus may easily consist of more than 16 bits and run at several hundred megahertz. In these systems, the receiving chip will have very specific setup and hold times. Violation of these timing requirements will result in system malfunction and may force the system clock frequency to be decreased. In this application, use of a deskewing system can guarantee that the timing requirements will be met. The skew between every bit and between the data bits and the transmitted clock can be programmed by the transmitting chip. Having a guaranteed maximum skew between the bits allows more flexibility in determining the system timing margins. Reducing the allocation for skew in the timing margins allows the bus to run at a higher frequency.

With the increasing popularity of differential signalling techniques, such as low voltage differential signalling (LVDS), and the widespread use presently of these techniques, use of the differential deskewing system has many applications. Any differential signalling technique is sensitive to skew between the traces. Common differential systems include twisted pair LAN cables and many clock distribution systems.

7.4 Contributions

The key contributions of this work are:

1. An open-loop deskewing system.

    - Development of an open-loop architecture for deskewing wide data buses.

The system uses TDR to eliminate the need for dummy traces and can be applied to an arbitrary number of lines. Trace delay measurement and correction occurs in a single pulse.

- Presentation of an eight-line implementation of the open-loop architecture and validation of the architecture through experimental measurement in a 0.25 μm process.
- An extensive analysis and characterization of this implementation of the open-loop deskewing system with respect to delay, duty cycle distortion, conversion time, resolution, and noise margins.
- Derivation of a simple equation for predicting the magnitude of overshoot at the output node of a chip.
- Derivation of a simple model for predicting the effects of capacitive terminations on deskewing systems utilizing TDR techniques. Validation of the model was performed in simulation using the open-loop deskewing system.
- An extensive analysis of the performance limitations of the open-loop deskewing architecture.
- An investigation of the impact of inductive coupling on the the performance of the open-loop deskewing system.

2. A differential deskewing system.

- Development of a DLL based architecture for deskewing a differential pair of PCB traces. The simple TDR techniques used previously were extended to work for a pair of lines with a series termination.
- Presentation of an implementation of the differential deskewing architecture and validation of the architecture through experimental measurement in a 0.25 μm process.

- An extensive analysis and characterization of this implementation of the differential deskewing system.

3. A current-based deskewing system.

   - Development of an architecture utilizing output driver current levels to deskew a wide data bus.
   - Presentation of a simple implementation of the current-based deskewing system and validation based on simulation results in a 0.25 μm process.
   - Comparison of the current-based deskewing architecture to voltage-based architectures.

7.5 Future Work

Based on the work presented here, there exist several potential directions for future research. The first extension of this work is to apply the differential deskewing architecture to a bus of differential lines. This can be achieved by simply using a set of DLL's to align every negative PCB trace to one trace chosen to be a reference. After every negative trace is aligned, the differential architecture presented here can be used to align the positive traces to the negative traces.

Another extension of this work is to develop an open-loop differential deskewing system. Combining the delay measurement technique from the open-loop system with the TDR techniques from the differential system directly leads to an open-loop differential system.

Another future research area is developing a technique to automatically detect which trace in a differential pair is the longer. This can be easily achieved by a comparison from a single pulse. Use of this would eliminate the need to add an extra offset to the negative PCB trace to allow for the possibility that the negative trace is shorter than the positive trace. Without the offset delay, the full scale range of the

differential deskewing system can be doubled.

Future research efforts can also focus on optimization of the systems presented here. Several parameters that could be improved include offset delay, power consumption, and duty cycle distortion. The open-loop deskewing system's sensitivity to process variations could be reduced by making the delay stages identical to oscillator stages. This would allow the delay per stage for the VCDL and the oscillator to track each other across process corners.

Another possible area for research is application of the techniques presented here to development of deskewing input buffers. Instead of measuring the trace delay from the transmitting chip, the receiving chip could measure the trace delay and then adjust the delay at the chip input to compensate for signal skew. Development of this system will require only minor modification of the architectures presented here.

APPENDIX A

COEFFICIENT DERIVATION

A.1 Derivation

Beginning from Equation 27, which is replicated here, all the unknown coefficients can be determined.

$$V_{p0}(s) = \frac{1}{4}\frac{L_P - R_s^2 C_P}{R_s}\frac{1}{s} + \frac{1}{2}\frac{1}{s^2} - \frac{1}{4R_s}\frac{2R_s^2 L_p C_p + L_p^2 - R_s^4 C_p^2 + s(R_s L_p^2 C_p - R_s^3 L_p C_p^2)}{2R_s + sL_p + +sR_s^2 C_p + s^2(R_s L_p C_p)} \tag{117}$$

The inverse Laplace transform of the first two terms is trivial. The remaining coefficients are found through a straightforward, although more complicated approach. From the form of the third term of Equation 117, it is know the form of the transform will be

$$-\frac{1}{4R_s}\frac{2R_s^2 L_p C_p + L_p^2 - R_s^4 C_p^2 + s(R_s L_p^2 C_p - R_s^3 L_p C_p^2)}{2R_s + sL_p + +sR_s^2 C_p + s^2(R_s L_p C_p)} \leftrightarrow C_1\, e^{-at} cos(\omega t) + C_2\, e^{-at} sin(\omega t) \tag{118}$$

Therefore, the final term in Equation 117 must be rearranged into the form of the left hand side of Equation 118. This is the starting point of the derivation and is shown below.

$$-\frac{1}{4R_s}\frac{2R_s^2 L_p C_p + L_p^2 - R_s^4 C_p^2 + s(R_s L_p^2 C_p - R_s^3 L_p C_p^2)}{2R_s + sL_p + +sR_s^2 C_p + s^2(R_s L_p C_p)} = \frac{C_1(s+a)}{(s+a)^2 + w^2} + \frac{C_2\,\omega}{(s+a)^2 + \omega^2} \tag{119}$$

Examination of this equation shows that C_1 will be the coefficient of the s order term in the numerator, and will be given by:

$$C_1 = -\frac{1}{4R_s}\left(\frac{R_s^2 L_p C_p - R_s^3 L_p C_p}{R_s L_p C_p}\right) \tag{120}$$

$$C_1 = \frac{1}{4}\left(R_s C_p - \frac{L_p}{R_s}\right) \tag{121}$$

Comparison of the denominators of Equation 119 gives

$$(s+a)^2+\omega^2 = s^2+2as+a^2+\omega^2 = s^2+s\Big(\frac{L_p+R_s^2C_p}{R_sL_pC_p}\Big)+\frac{2R_s}{R_sL_pC_p} \tag{122}$$

Comparing terms with the same magnitude of s gives:

$$2as = \frac{L_p+R_s^2C_p}{R_sL_pC_p} \tag{123}$$

$$a^2+\omega^2 = \frac{2R_s}{R_sL_pC_p} \tag{124}$$

Equation 123 can easily be solved to give

$$a = \frac{1}{2}\frac{L_p+R_s^2C_p}{R_sL_pC_p} \tag{125}$$

Equation 124 can then be solved to give

$$\omega = \sqrt{\frac{2R_s}{R_sL_pC_p}-a^2} \tag{126}$$

$$\omega = \sqrt{\frac{2R_s}{R_sL_pC_p}-\frac{1}{4}\frac{L_p^2+2R_s^2L_pC_p+R_s^4C_p^2}{R_s^2L_p^2C_p^2}} \tag{127}$$

$$\omega = \sqrt{\frac{2R_s^2LC-1/4L^2-1/2R_s^2LC-1/4R_s^4C^2}{R_s^2L^2C^2}} \tag{128}$$

$$\omega = \frac{1}{2}\sqrt{\frac{6R_s^2L_pC_p-L_p^2-R_s^4C_p^2}{R_s^2L_p^2C_p^2}} \tag{129}$$

The remaining unknown, C_2, must then be calculated. To do this, the numerator terms of Equation 119 are compared, giving

$$C_1a+C_2\omega = -\frac{1}{4R_s}\frac{2R_s^2L_pC_p+L_p^2-R_s^4C_p^2}{R_sL_pC_p} \tag{130}$$

Substituting back the expressions for C_1 and a gives

$$\frac{1}{4}\Big(\frac{R_s^2C_p-L_p}{4R_s}\Big)\frac{1}{2}\frac{L_p+R_s^2C_p}{R_sL_pC_p}+C_2\omega = -\frac{1}{4R_s}\frac{2R_s^2L_pC_p+L_p^2-R_s^4C_p^2}{R_sL_pC_p} \tag{131}$$

$$\frac{R_s^4C_p^2-L_p^2}{8R_s^2L_pC_p}+C_2\omega = \frac{-4R_s^2L_pC_p-2L_p^2+2R_s^4C_p^2}{8R_s^2L_pC_p} \tag{132}$$

$$C_2\omega = \frac{-4R_s^2L_pC_p - 2L_p^2 + 2R_s^4C_p^2 - R_s^4C_p^2 + L_p^2}{8R_s^2L_pC_p} \tag{133}$$

$$C_2\omega = \frac{R_s^4C_p^2 - 4R_s^2L_pC_p - L_p^2}{8R_s^2L_pC_p} \tag{134}$$

$$C_2 = \frac{1}{8\omega}\frac{R_s^4C_p^2 - 4R_s^2L_pC_p - L_p^2}{R_s^2L_pC_p} \tag{135}$$

These results are further simplified to give:

$$a = \frac{1}{2}\left(\frac{1}{R_sC_p} + \frac{R_s}{L_p}\right) \tag{136}$$

$$\omega = \frac{1}{2}\sqrt{\frac{6}{L_pC_p} - \frac{1}{R_s^2C_p^2} - \frac{R_s^2}{L_p^2}} \tag{137}$$

$$C_1 = \frac{1}{4}\left(R_sC_p - \frac{L_p}{R_s}\right) \tag{138}$$

$$C_2 = \frac{1}{8\omega}\left(\frac{R_s}{L_p}R_sC_p - \frac{L_p}{R_s}\frac{1}{R_sC_p} - 4\right) \tag{139}$$

REFERENCES

[1] Balatsos, A. and Lewis, D., "Low-skew clock generator with dynamic impedance and delay matching," in *ISSCC Dig. Technical Papers*, vol. 1, (San Francisco, CA), pp. 182 – 183, 1999.

[2] Bertin, C. L., "Transmission-line response using frequency techniques," *IBM J. Res. Develop.*, pp. 52–63, Jan. 1964.

[3] Brueske, D. and Embabi, S., "A dynamic clock synchronization technique for large systems," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 17, pp. 350 – 361, Aug. 1994.

[4] Chae, J., Kim, D., and Kim, D., "Wide range single-way-pumping synchronous mirror delay," *Electronics Letters*, vol. 36, pp. 939–940, May 2000.

[5] Davis, J. A. and Meindl, J. D., "Compact distributed rlc interconnect models - part 1: Single line transient, time delay, and overshoot expressions," *IEEE Trans. Electron Devices*, vol. 47, pp. 2068 – 2077, Nov. 2000.

[6] Davis, J. A. and Meindl, J. D., "Compact distributed rlc interconnect models - part 2: Coupled line transient expressions and peak crosstalk in multilevel networks," *IEEE Trans. Electron Devices*, vol. 47, pp. 2078 – 2087, Nov. 2000.

[7] Dehng, G., Hsu, J., Yang, C., and Liu, S., "Clock-deskew buffer using a sar-controlled delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1128–1136, Aug. 2000.

[8] Deutsch, A., Kopcsay, G. V., Ranieri, V. A., Cataldo, J. K., Galligan, E. A., Graham, W. S., Graham, R. P., McGouey, R. P., Nunes, S. L., Paraszczak, J. R., Ritsko, J. J., Serino, R. J., Shih, D. Y., and Wilczynski, J. S., "High-speed signal propagation on lossy tranmission lines," *IBM J. Res. Develop.*, vol. 34, pp. 601–615, 1990.

[9] Eken, Y. A., *High Frequency Voltage Controlled Ring Oscillators in Standard CMOS*. GA, USA: Ph.D. Dissertation, Georgia Institute of Technology, 2003.

[10] Gentili, G. G. and Melloni, A., "The incremental inductance rule in quasi-tem coupled transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 1276–1280, 1995.

[11] Gneiting, T. and Jalowiecki, I., "Influence of process parameter variations on the signal distribution behavior of wafer scale integration devices," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 18, pp. 424–430, Aug. 1995.

[12] Grover, F. W., *Inductance Calculations*. NY, USA: D. Van Nostrand Company, Inc., second ed., 1946.

[13] Horowitz, M., "Clocking strategies and high-performance processors," in *Proc. IEEE Int. Symp. VLSI Circuits*, pp. 50 – 53, 1992.

[14] Jang, S., "A new synchronous mirror delay with an auto-skew-generation circuit," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. 397 –400, 2003.

[15] Jang, S., Jun, Y., Lee, J., and Kong, B., "Asmd with duty cycle correction scheme for high-speed dram," *Electronics Letters*, vol. 37, pp. 1004–1006, Aug. 2001.

[16] Johnson, H. and Graham, M., *High-Speed Signal Propagation - Advanced Black Magic*. Upper Saddle River, NJ, USA: Prentice Hall, first ed., 2003.

[17] Johnson, M. and Hudson, E., "A variable delay line pll for cpu-coprocessor synchronization," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1218–1223, Oct. 1995.

[18] Kim, T., Wang, S., and Kim, B., "A low jitter, fast locking delay locked loop using measure and control scheme," in *Proc. IEEE Midwest Symp. Mixed Signal Design*, pp. 45 –50, 2001.

[19] Knight, T. and Wu, H., "A method for skew-free distribution of digital signals using matched variable delay lines," in *Proc. IEEE Int. Symp. VLSI Circuits*, pp. 19–20, 1993.

[20] Kraus, J. D. and Fleisch, D. A., *Electromagnetics with Applications*. Boston, MA, USA: McGraw Hill, fifth ed., 1999.

[21] Liu, S., Lee, J., and Tsao, H., "Low-power clock-deskew buffer for high-speed digital circuits," *IEEE J. Solid-State Circuits*, vol. 34, pp. 554–558, 1999.

[22] Mullick, S. K., "Propagation of signals in nonlinear tranmission lines," *IBM J. Res. Develop.*, pp. 558–562, Sept. 1967.

[23] Pozar, D., *Microwave Engineering*. NY, USA: John Wiley and Sons, second ed., 1998.

[24] Saeki, T., Minami, K., Yoshida, H., and Suzuki, H., "The direct skew detect synchronous mirror delay (direct smd) for asics," in *Proc. IEEE Custom Integrated Circuits Conf.*, (CA), pp. 511–514, 1998.

[25] Saeki, T., Minami, K., Yoshida, H., and Suzuki, H., "A direct-skew-detect synchronous mirror delay for application specific integrated circuits," *IEEE J. Solid-State Circuits*, vol. 34, pp. 372–379, Mar. 1999.

[26] Saeki, T., Nakamura, H., and Shimizu, J., "A 10ps clock cycle lock time cmos digital clock generator based on an interleaved synchronous mirror delay scheme," in *Proc. IEEE Int. Symp. VLSI Circuits*, pp. 109–110, 1997.

[27] Saeki, T., Nakaoka, Y., Fujita, M., Tanaka, A., Nagata, K., Sakakibara, K., Matano, T., Hoshino, Y., Miyano, K., andS. Nakazawa, S. I., Kakehashi, E., Drynan, J., Komuro, M., Fukase, T., Iwasaki, H., Takenaka, M., Sekine, J., Igeta, M., Nakanishi, N., Itani, T., Yoshida, K., Yoshino, H., Hashimoto, S., Yoshii, T., Ichinose, M., Imura, T., Uziie, M., Kikuchi, S., Koyama, K., Fukuzo, Y., and Okuda, T., "A 2.5-ns clock access, 250-mhz, 256-mb sdram with synchronous mirror delay," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1656–1668, Nov. 1996.

[28] Shim, D., Jung, Y., Lee, S., , and Kim, W., "Fast locking clock generator using analog synchronous mirror delay technique with feedback control," in *International Conference on Solid-State and Integrated-Circuit Technology*, vol. 2, pp. 1125 –1127, 2001.

[29] Shim, D., Lee, D., Jung, S., Kim, C., and Kim, W., "An analog synchronous mirror delay for high-speed dram application," *IEEE J. Solid-State Circuits*, vol. 34, pp. 484–493, 1999.

[30] Sohn, Y., Lee, J., Park, H., and Cho, S., "Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board," *IEEE Trans. Adv. Packag.*, vol. 24, pp. 521–527, Nov. 2001.

[31] Sun, L., Kwasniewski, T., and Iniewski, K., "A quadrature output voltage controlled ring oscillator based on three-stage subfeedback loops," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, (Orlando, FL), pp. 176–179, 1999.

[32] Sung, K., Yang, B., , and Kim, L., "Low power clock generator based on an area-reduced interleaved synchronous mirror delay scheme," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, pp. 671–674, 2002.

[33] Sung, K., Yang, B., and Kim, L., "Low power clock generator based on an area-reduced interleaved synchronous mirror delay scheme," *Electronics Letters*, vol. 38, pp. 399–400, 2002.

[34] Sutoh, H., Yamakoshi, K., and Ino, M., "Circuit technique for skew-free clock distribution," in *Proc. IEEE Custom Integrated Circuits Conf.*, vol. 1, (Santa Clara, CA USA), pp. 163–166, 1995.

[35] Tam, S., Rusu, S., Desai, U., Kim, R., Zhang, J., and Young, I., "Clock generation and distribution for the first ia-64 microprocessor," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1545–1552, Nov. 2000.

[36] Tan, G., Surparjo, B., Wagiran, R., and Sidek, R., "The design of 8-bit cmos digital to analog converter," in *IEEE Int. Conf. on Semiconductor Electronics*, pp. 231–234, Nov. 2000.

[37] Tanoi, S., Tanabe, T., Takahashi, K., Miyamoto, S., and Uesugi, M., "A 250-622 mhz deskew and jitter-suppressed clock buffer using two-loop architecture," *IEEE J. Solid-State Circuits*, vol. 31, pp. 487–493, 1996.

[38] Uyemura, J., *CMOS Logic Circuit Design*. Boston, MA, USA: Kluwer Academic Publishers, 1999.

[39] Watson, R. and Iknaian, R., "Clock buffer chip with multiple target automatic skew compensation," *IEEE J. Solid-State Circuits*, vol. 301, pp. 1267–1276, Nov. 1995.

[40] Yang, C. and Liu, S., "A one-wire approach for skew-compensating clock distribution based on bidirectional techniques," *IEEE J. Solid-State Circuits*, vol. 36, pp. 266–272, Feb. 2001.

[41] Yeung, E. and Horowitz, M., "A 2.4 gb/s/pin simultaneous bidirectional parallel link with per-pin skew compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1619–1628, Nov. 2000.

VITA

Amer Hani Atrash was born in Atlanta, GA in 1981. He received his B.S. degree in electrical engineering from the Georgia Institute of Technology in 2001 and his M.S. degree in electrical engineering from the same university in 2002.

His interest in integrated circuit design started with work on current-mode logic (CML) circuits in Dr. Uyemura's group during his first year of graduate studies. This work involved design and characterization of CML circuits and comparison to static CMOS techniques in a multiplier application with the ultimate goal of developing a 10 GHz serializer/deserializer in a 0.13 μm process.

The work in CML circuits evolved into design of a VCDL which led to the study of deskewing systems, in close collaboration with Dr. Brian Butka of Integrated Device Technology. Several deskewing architectures were examined and implemented in a 0.25 μm technology, covering both single-ended and differential signalling systems.